

Comlinear™ CLC2600, CLC3600, CLC4600

Dual, Triple, and Quad 300MHz Amplifiers



FEATURES

- 0.1dB gain flatness to 95MHz
- 0.03%/0.04° differential gain/phase error
- 230MHz -3dB bandwidth at G = 2
- 300MHz -3dB bandwidth at G = 1
- 1,300V/μs slew rate
- 50mA output current (easily drives two video loads)
- 3.3mA supply current
- Fully specified at ±5V supplies
- CLC2600: Lead-free SOIC-8
- CLC4600: Lead-free SOIC-14

APPLICATIONS

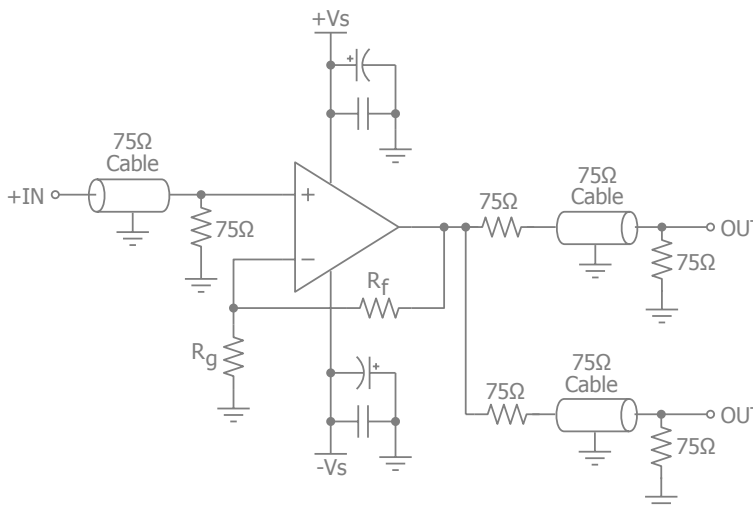
- Video line drivers
- S-Video driver
- Video switchers and routers
- ADC buffer
- Active filters
- Cable drivers
- Twisted pair driver/receiver

General Description

The *Comlinear* CLC2600 (dual), CLC3600 (triple), and CLC4600 (quad) are high-performance, current feedback amplifiers. These amplifiers provide 300MHz unity gain bandwidth, ±0.1dB gain flatness to 95MHz, and provide 1,300V/μs slew rate exceeding the requirements of high-definition television (HDTV) and other multimedia applications. These *Comlinear* high-performance amplifiers also provide ample output current to drive multiple video loads.

The *Comlinear* CLC2600, CLC3600, and CLC4600 are designed to operate from ±5V supplies. They consume only 3.3mA of supply current per channel. The combination of high-speed, low-power, and excellent video performance make these amplifiers well suited for use in many general purpose, high-speed applications including standard definition and high definition video.

Typical Application - Driving Dual Video Loads



Ordering Information

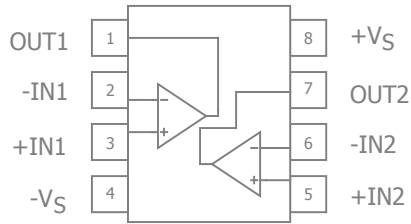
Part Number	Package	Pb-Free	Operating Temperature Range	Packaging Method
CLC2600IM8X	SOIC-8	Yes	-40°C to +85°C	Reel
CLC2600IM8	SOIC-8	Yes	-40°C to +85°C	Rail
CLC3600IM14X	SOIC-14	Yes	-40°C to +85°C	Reel
CLC3600IM14	SOIC-14	Yes	-40°C to +85°C	Rail
CLC4600IM14X	SOIC-14	Yes	-40°C to +85°C	Reel
CLC4600IM14	SOIC-14	Yes	-40°C to +85°C	Rail

Moisture sensitivity level for all parts is MSL-1.

Comlinear™ CLC2600, CLC3600, CLC4600 Dual, Triple, and Quad 300MHz Amplifiers REV 0.1.2



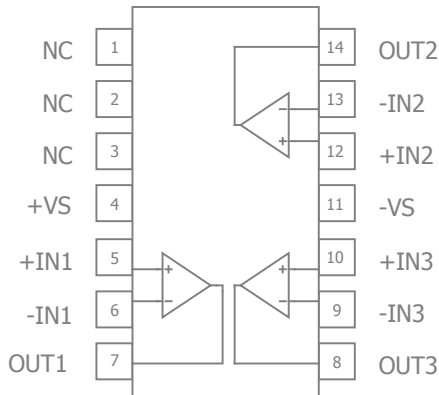
CLC2600 Pin Configuration



CLC2600 Pin Assignments

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	-VS	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	+VS	Positive supply

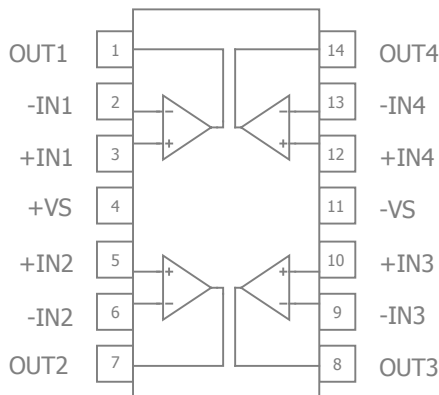
CLC3600 Pin Configuration



CLC3600 Pin Configuration

Pin No.	Pin Name	Description
1	NC	No Connect
2	NC	No Connect
3	NC	No Connect
4	+VS	Positive supply
5	+IN1	Positive input, channel 1
6	-IN1	Negative input, channel 1
7	OUT1	Output, channel 1
8	OUT3	Output, channel 3
9	-IN3	Negative input, channel 3
10	+IN3	Positive input, channel 3
11	-VS	Negative supply
12	+IN2	Positive input, channel 2
13	-IN2	Negative input, channel 2
14	OUT2	Output, channel 2

CLC4600 Pin Configuration



CLC4600 Pin Configuration

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	+VS	Positive supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	OUT3	Output, channel 3
9	-IN3	Negative input, channel 3
10	+IN3	Positive input, channel 3
11	-VS	Negative supply
12	+IN4	Positive input, channel 4
13	-IN4	Negative input, channel 4
14	OUT4	Output, channel 4



Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Parameter	Min	Max	Unit
Supply Voltage	0	14	V
Input Voltage Range	$-V_S - 0.5V$	$+V_S + 0.5V$	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Package Thermal Resistance				
8-Lead SOIC		TBD		°C/W
14-Lead SOIC		TBD		°C/W

Notes:

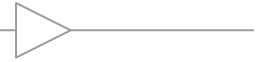
Package thermal resistance (θ_{JA}), JEDEC standard, multi-layer test boards, still air.

ESD Protection

Product	SOIC-8	SOIC-14
Human Body Model (HBM)	2kV	2kV
Charged Device Model (CDM)	TBD	TBD

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	± 4		± 6	V



Electrical Characteristics

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 510\Omega$, $R_L = 100\Omega$, $G = 2$; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	$G = +1$, $V_{OUT} = 0.2V_{pp}$, $R_f = 1.24k\Omega$		300		MHz
BW _{SS}	-3dB Bandwidth	$G = +2$, $V_{OUT} = 0.2V_{pp}$		230		MHz
BW _{LS}	Large Signal Bandwidth	$G = +2$, $V_{OUT} = 4V_{pp}$		155		MHz
BW _{0.1dBSS}	0.1dB Gain Flatness	$G = +2$, $V_{OUT} = 0.2V_{pp}$		95		MHz
BW _{0.1dBLS}	0.1dB Gain Flatness	$G = +2$, $V_{OUT} = 4V_{pp}$		55		MHz
Time Domain Response						
t_R , t_F	Rise and Fall Time	$V_{OUT} = 2V$ step; (10% to 90%)		1.8		ns
t_S	Settling Time to 0.1%	$V_{OUT} = 2V$ step		6		ns
OS	Overshoot	$V_{OUT} = 0.2V$ step		2.5		%
SR	Slew Rate	4V step		1300		V/ μ s
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	$2V_{pp}$, 1MHz		-80		dBc
HD3	3rd Harmonic Distortion	$2V_{pp}$, 1MHz		-86		dBc
THD	Total Harmonic Distortion	$2V_{pp}$, 1MHz		-79.5		dB
D _G	Differential Gain	NTSC (3.58MHz), DC-coupled, $R_L = 150\Omega$		0.03		%
D _P	Differential Phase	NTSC (3.58MHz), DC-coupled, $R_L = 150\Omega$		0.04		°
e_n	Input Voltage Noise	> 1MHz		6.4		nV/ $\sqrt{\text{Hz}}$
i_{n+}	Input Current Noise (+)	> 1MHz		1.0		pA/ $\sqrt{\text{Hz}}$
i_{n-}	Input Current Noise (-)	> 1MHz		9.3		pA/ $\sqrt{\text{Hz}}$
X _{TALK}	Crosstalk	Channel-to-channel 5MHz		-56		dB
DC Performance						
V_{IO}	Input Offset Voltage ⁽¹⁾		-6	1.4	+6	mV
dV_{IO}	Average Drift			15		$\mu\text{V}/^\circ\text{C}$
I_{bn}	Input Bias Current Non-inverting ⁽¹⁾		-2.6	1.3	2.6	μA
dI_{bn}	Average Drift			2.6		nA/ $^\circ\text{C}$
I_{bi}	Input Bias Current Inverting ⁽¹⁾		-14	4.4	14	μA
dI_{bni}	Average Drift			16		nA/ $^\circ\text{C}$
PSRR	Power Supply Rejection Ratio ⁽¹⁾	DC	63	65		dB
A _{OL}	Open-Loop Transresistance	$V_{OUT} = V_S / 2$		TBD		m Ω
I_S	Supply Current ⁽¹⁾	per channel		3.3	4.5	mA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		19		M Ω
C_{IN}	Input Capacitance			1		pF
CMIR	Common Mode Input Range			± 2.3		V
CMRR	Common Mode Rejection Ratio ⁽¹⁾	DC	54	57		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		110		m Ω
V_{OUT}	Output Voltage Swing	$R_L = 100\Omega$ ⁽¹⁾	-2.7	± 3	2.7	V
		$R_L = 1k\Omega$		± 3.3		V
I_{OUT}	Output Current			50		mA
I_{SC}	Short-Circuit Output Current	$V_{OUT} = V_S / 2$		67		mA

Notes:

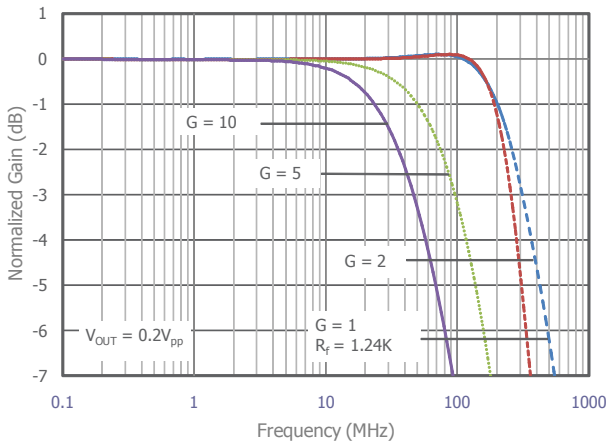
- 100% tested at 25°C



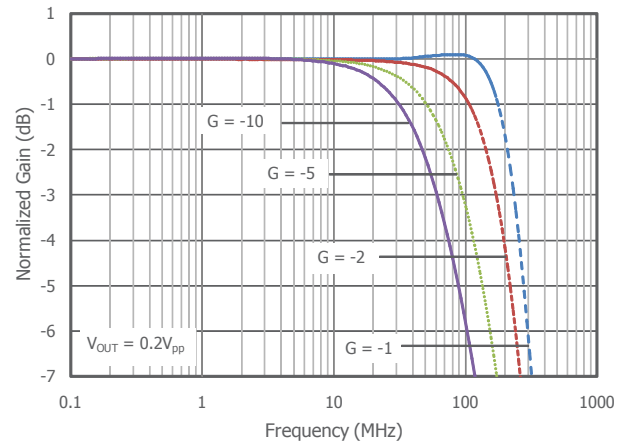
Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 510\Omega$, $R_L = 100\Omega$, $G = 2$; unless otherwise noted.

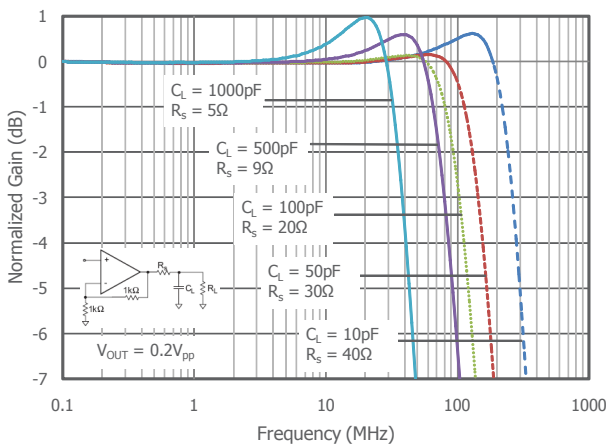
Non-Inverting Frequency Response



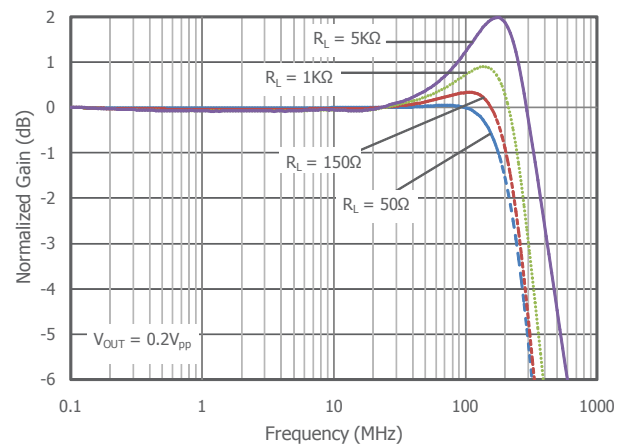
Inverting Frequency Response



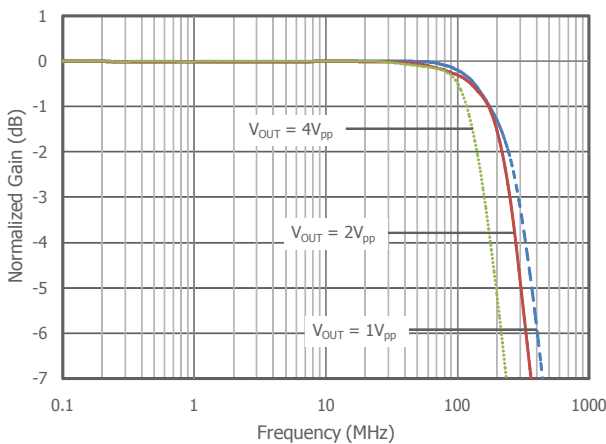
Frequency Response vs. C_L



Frequency Response vs. R_L



Frequency Response vs. V_{OUT}



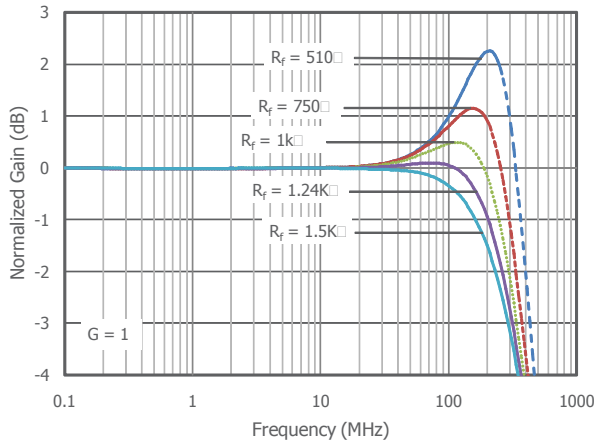
Frequency vs. Temperature



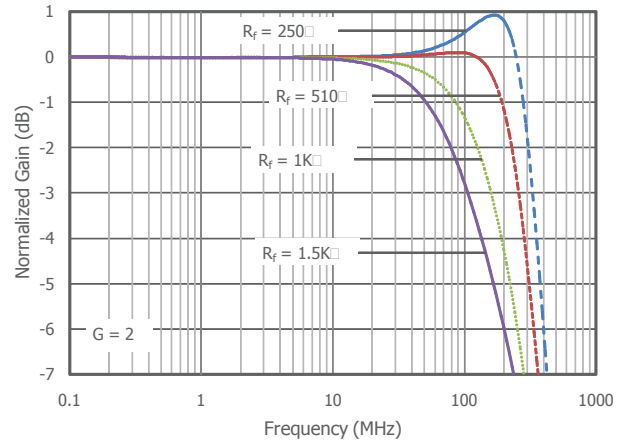
Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 510\Omega$, $R_L = 100\Omega$, $G = 2$; unless otherwise noted.

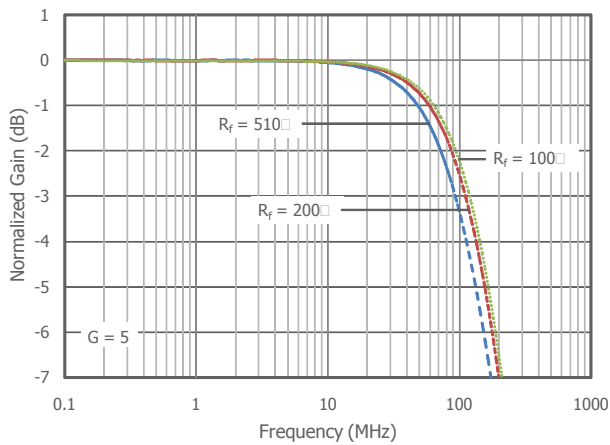
Frequency Response vs. R_f at $G=1$



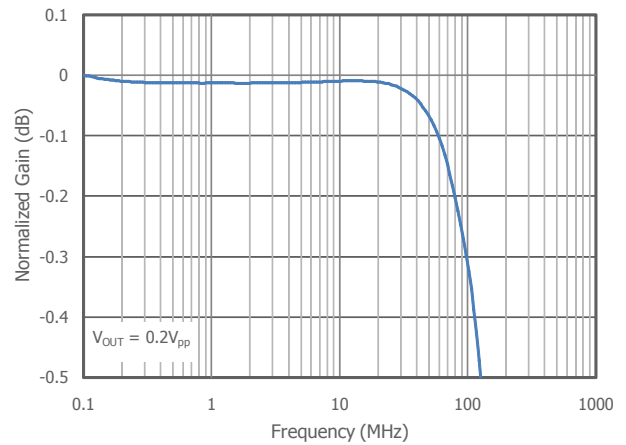
Frequency Response vs. R_f at $G=2$



Frequency Response vs. R_f at $G=5$



Gain Flatness



Open Loop Transimpedance Gain/Phase vs. Frequency

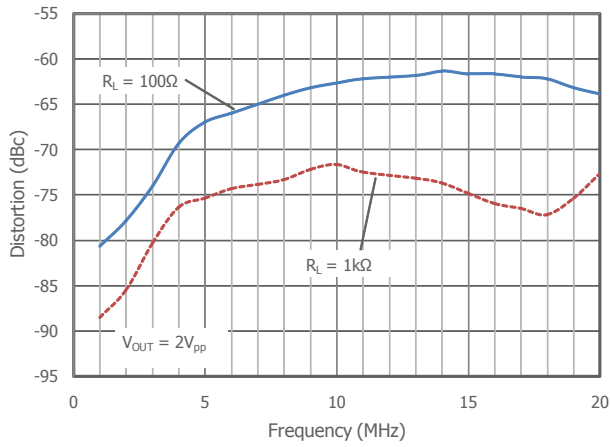
Input Voltage Noise



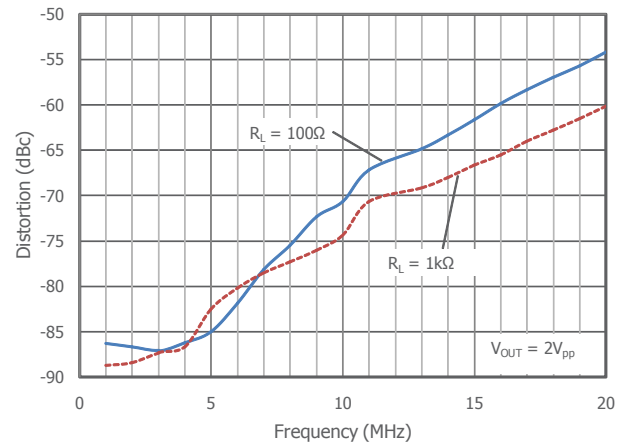
Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 510\Omega$, $R_L = 100\Omega$, $G = 2$; unless otherwise noted.

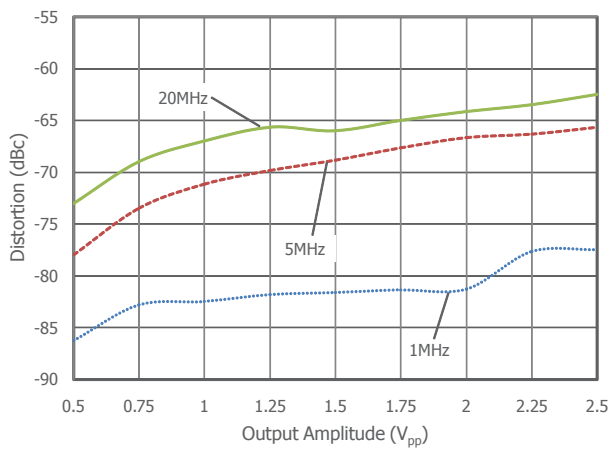
2nd Harmonic Distortion vs. R_L



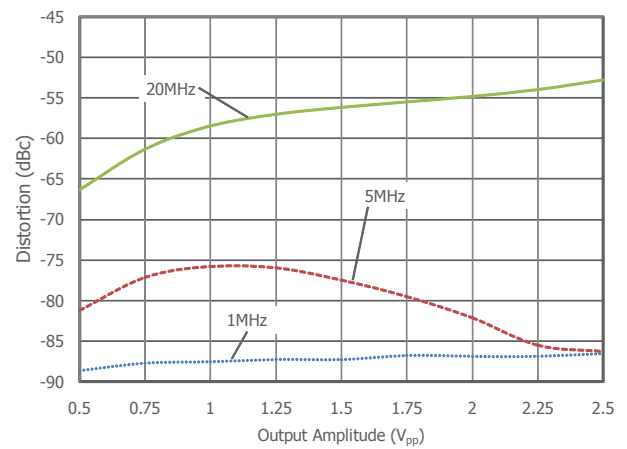
3rd Harmonic Distortion vs. R_L



2nd Harmonic Distortion vs. V_{OUT}



3rd Harmonic Distortion vs. V_{OUT}



CMRR vs. Frequency

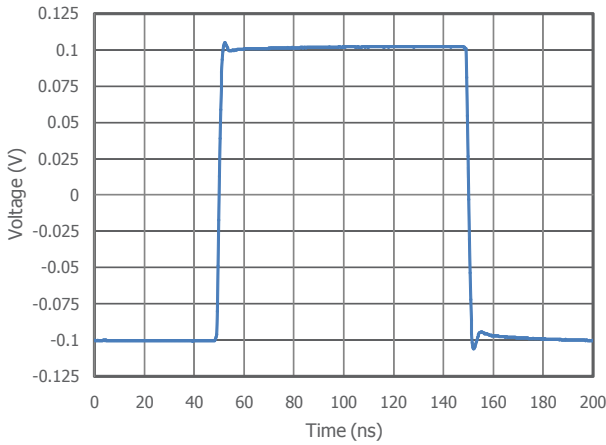
PSRR vs. Frequency



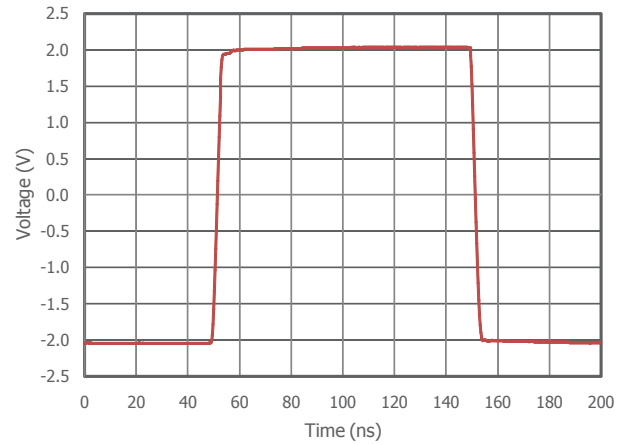
Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_f = 510\Omega$, $R_L = 100\Omega$, $G = 2$; unless otherwise noted.

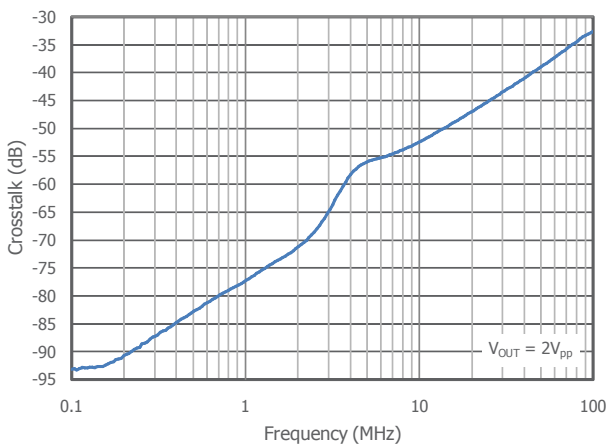
Small Signal Pulse Response



Large Signal Pulse Response

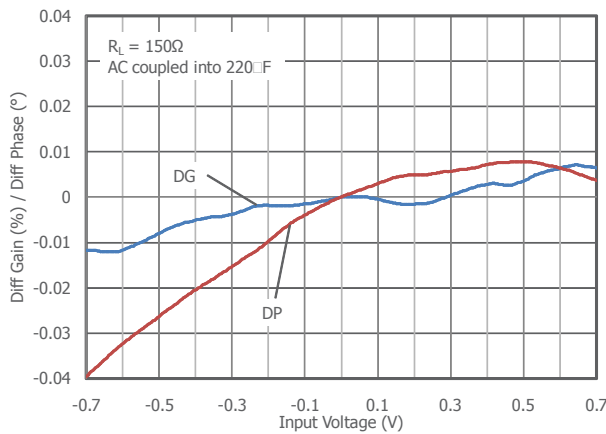


Crosstalk vs. Frequency

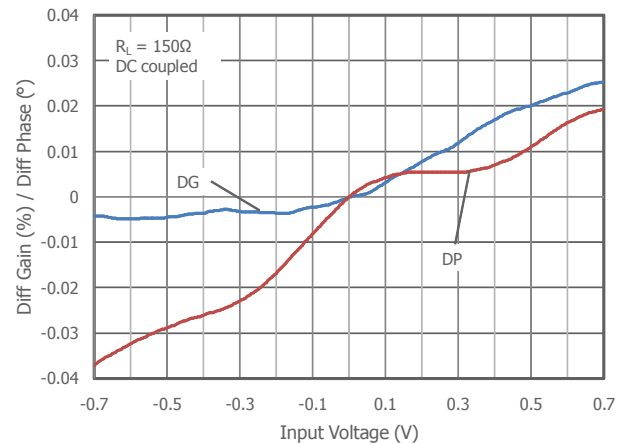


Closed Loop Output Impedance vs. Frequency

Differential Gain & Phase AC Coupled



Differential Gain & Phase DC Coupled





Application Information

Driving Capacitive Loads

The Frequency Response vs. C_L plot on page 5, illustrates the response of the CLCx600 Family. A small series resistance (R_S) at the output of the amplifier, illustrated in Figure 1, will improve stability and settling performance. R_S values in the Frequency Response vs. C_L plot were chosen to achieve maximum bandwidth with less than 1dB of peaking. For maximum flatness, use a larger R_S .

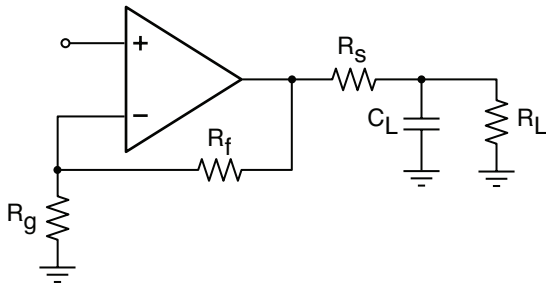


Figure 1. Typical Topology for Driving Capacitive Loads

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C for an extended time, device failure may occur. The CLCx600 are short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. RMS Power Dissipation can be calculated using the following equation:

$$\text{Power Dissipation} = I_S * (V_{S+} - V_{S-}) + (V_{S+} - V_O(\text{RMS})) * I_{OUT}(\text{RMS})$$

Where I_S is the supply current, V_{S+} is the positive supply pin voltage, V_{S-} is the negative supply pin voltage, $V_O(\text{RMS})$ is the RMS output voltage and $I_{OUT}(\text{RMS})$ is the RMS output current delivered to the load. Follow the maximum power derating curves shown in Figure 2 to ensure proper operation.

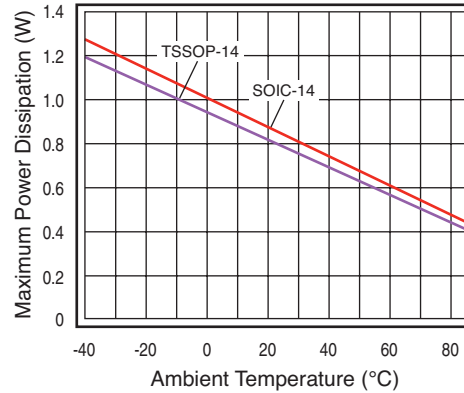


Figure 2. Maximum Power Derating

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The CLCx600 Family will typically recover in less than 20ns from an overdrive condition. Figure 3 shows the CLC2600 in an overdriven condition.

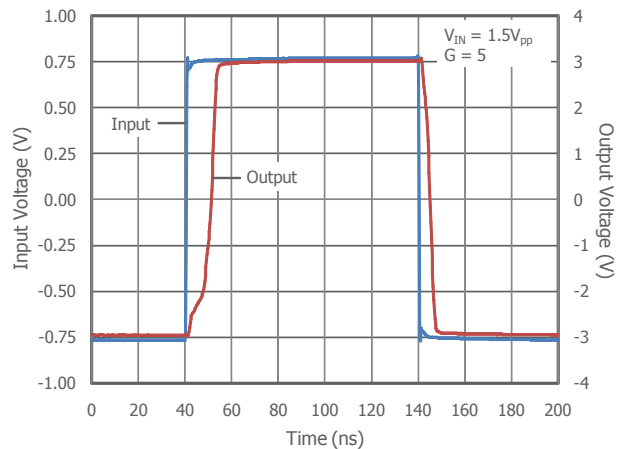


Figure 3. Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Fairchild has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.01μF ceramic capacitors
- Place the 6.8μF capacitor within 0.75 inches of the power pin



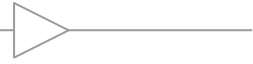
- Place the 0.01 μ F capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

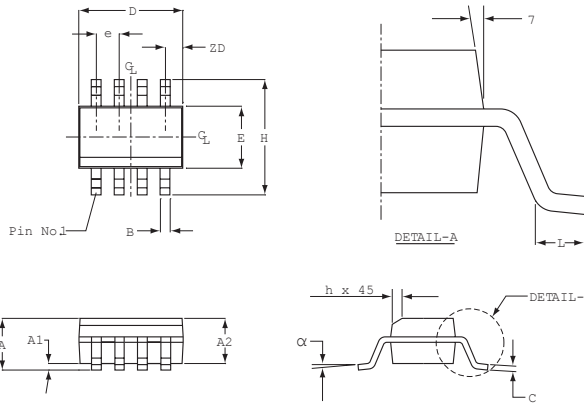
The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board Schematics



Mechanical Dimensions

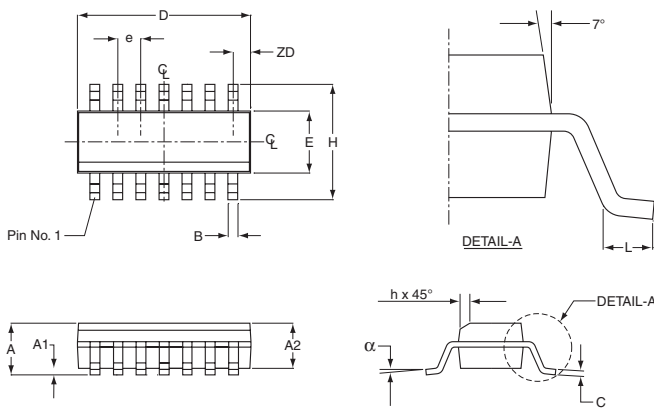
SOIC-8 Package



SOIC-8		
SYMBOL	MIN	MAX
A1	0.0	0.25
B	0.36	0.4
C	0.3	0.25
D	4.20	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.52	1.72
ZD	0.5 ref	
A2	1.37	1.57

- NOTE:
1. All dimensions are in millimeters.
 2. Lead coplanarity should be 0 to 0.1mm (.004") max.
 3. Package surface finishing:
 - (1) Top: matte (charmilles #18-30).
 - (2) All sides: matte (charmilles #18-30).
 - (3) Bottom: smooth or matte (charmilles #18-30).
 4. All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.15mm (.006) per side (D).

SOIC-14 Package



SOIC-14		
SYMBOL	MIN	MAX
A1	.0040	.0098
B	.014	.018
C	.0075	.0098
D	.337	.344
E	.150	.157
e	.050 BSC	
H	.2284	.2440
h	.0099	.0196
L	.016	.050
A	.060	.068
ZD	0° 8°	
A2	.054	.062

- NOTE:
1. All dimensions are in inches.
 2. Lead coplanarity should be 0 to 0.10mm (.004") max.
 3. Package surface finishing:
 - (1) Top: matte (charmilles #18-30).
 - (2) All sides: matte (charmilles #18-30).
 - (3) Bottom: smooth or matte (charmilles #18-30).
 4. All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.152mm (.006) per side (D).

For additional information regarding our products, please visit the CADEKA at: cadeka.com

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