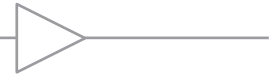


Comlinear[®] CLC1605, CLC3605

Single and Triple, 1.4GHz Amplifiers



FEATURES

- 0.1dB gain flatness to 120MHz
- 0.02%/0.02° differential gain/phase
- 1.4GHz -3dB bandwidth at G = 2
- 650MHz large signal bandwidth
- 2,500V/μs slew rate
- 5nV/√Hz input voltage noise
- 120mA output current
- Triple offers disable
- Fully specified at 5V and ±5V supplies
- CLC1605: Pb-free SOT23-5
- CLC3605: Pb-free SOIC-16

APPLICATIONS

- RGB video line drivers
- High definition video driver
- Video switchers and routers
- ADC buffer
- Active filters
- High-speed instrumentation
- Wide dynamic range IF amp
- Radar/communication receivers

General Description

The *Comlinear* CLC1605 (single) and CLC3605 (triple) are high-performance, current feedback amplifiers that provide 1.4GHz gain of 2 bandwidth, ±0.1dB gain flatness to 120MHz, and 2,500V/μs slew rate. This high performance exceeds the requirements of high-definition television (HDTV) and other multimedia applications. These *Comlinear* high-performance amplifiers also provide ample output current to drive multiple video loads.

The *Comlinear* CLC1605 and CLC3605 are designed to operate from ±5V or +5V supplies. The CLC3605 offers a fast enable/disable feature to save power. While disabled, the outputs are in a high-impedance state to allow for multiplexing applications. The combination of high-speed, low-power, and excellent video performance make these amplifiers well suited for use in many general purpose, high-speed applications including high-definition video, imaging applications, and radar/communications receivers.

Typical Application - TBD

Ordering Information

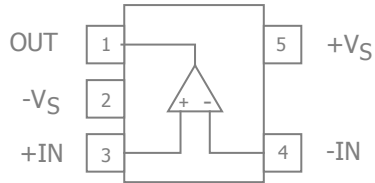
Part Number	Package	Pb-Free	Operating Temperature Range	Packaging Method
CLC1605IST6X	SOT23-5	Yes	-40°C to +85°C	Reel
CLC3605ISO16X*	SOIC-16	Yes	-40°C to +85°C	Reel
CLC3605ISO16*	SOIC-16	Yes	-40°C to +85°C	Rail

*Preliminary Product Information

Moisture sensitivity level for all parts is MSL-1.



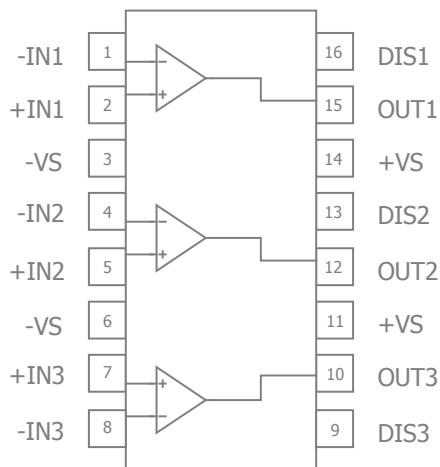
CLC1605 Pin Configuration



CLC1605 Pin Assignments

Pin No.	Pin Name	Description
1	OUT	Output
2	-VS	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	+VS	Positive supply

CLC3605 Pin Configuration



CLC3605 Pin Configuration

Pin No.	Pin Name	Description
1	-IN1	Negative input, channel 1
2	+IN1	Positive input, channel 1
3	-VS	Negative supply
4	-IN2	Negative input, channel 2
5	+IN2	Positive input, channel 2
6	-VS	Negative supply
7	+IN3	Positive input, channel 3
8	-IN3	Negative input, channel 3
9	DIS3	Disable pin. Enabled if pin is grounded, left floating or pulled below V_{ON} , disabled if pin is pulled above V_{OFF} .
10	OUT3	Output, channel 3
11	+VS	Positive supply
12	OUT2	Output, channel 2
13	DIS2	Disable pin. Enabled if pin is grounded, left floating or pulled below V_{ON} , disabled if pin is pulled above V_{OFF} .
14	+VS	Positive supply
15	OUT1	Output, channel 1
16	DIS1	Disable pin. Enabled if pin is grounded, left floating or pulled below V_{ON} , disabled if pin is pulled above V_{OFF} .

Disable Pin Truth Table

Pin	High	Low*
DIS	Disabled	Enabled

*Default Open State



Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	14	V
Input Voltage Range	$-V_S - 0.5V$	$+V_S + 0.5V$	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Package Thermal Resistance				
5-Lead SOT23		221		°C/W
16-Lead SOIC		68		°C/W

Notes:

Package thermal resistance (θ_{JA}), JEDEC standard, multi-layer test boards, still air.

ESD Protection

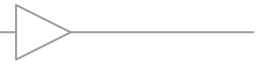
Product	SOT23-6	SOIC-16
Human Body Model (HBM)	2kV	2kV
Charged Device Model (CDM)	1kV	1kV

Notes:

0.8kV between the input pairs (+IN and -IN) pins only. All other pins are 2kV.

Recommended Operating Conditions

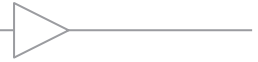
Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	4.5		12	V



Electrical Characteristics at +5V

$T_A = 25^\circ\text{C}$, $V_S = +5\text{V}$, $R_f = R_g = 330\Omega$, $R_L = 150\Omega$ to $V_S/2$, $G = 2$; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	Unity Gain Bandwidth	$G = +1$, $V_{OUT} = 0.5V_{pp}$, $R_f = xxx\Omega$		TBD		MHz
BW _{SS}	-3dB Bandwidth	$G = +2$, $V_{OUT} = 0.5V_{pp}$		800		MHz
BW _{LS}	Large Signal Bandwidth	$G = +2$, $V_{OUT} = 1V_{pp}$		450		MHz
BW _{0.1dBSS}	0.1dB Gain Flatness	$G = +2$, $V_{OUT} = 0.5V_{pp}$		100		MHz
BW _{0.1dBLS}	0.1dB Gain Flatness	$G = +2$, $V_{OUT} = 1V_{pp}$		TBD		MHz
Time Domain Response						
t_R , t_F	Rise and Fall Time	$V_{OUT} = 1\text{V}$ step; (10% to 90%)		1.2		ns
t_S	Settling Time to 0.1%	$V_{OUT} = 1\text{V}$ step		10		ns
OS	Overshoot	$V_{OUT} = 0.2\text{V}$ step		1		%
SR	Slew Rate	2V step		1500		V/ μs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	$V_{OUT} = 1V_{pp}$, 5MHz		-61		dBc
HD3	3rd Harmonic Distortion	$V_{OUT} = 1V_{pp}$, 5MHz		-61		dBc
THD	Total Harmonic Distortion	$V_{OUT} = 1V_{pp}$, 5MHz		58		dB
D _G	Differential Gain	NTSC (3.58MHz), DC-coupled, $R_L = 150\Omega$		0.02		%
D _P	Differential Phase	NTSC (3.58MHz), DC-coupled, $R_L = 150\Omega$		0.02		°
IP3	Third Order Intercept	$V_{OUT} = 0.5V_{pp}$, 10MHz		28		dBm
SFDR	Spurious Free Dynamic Range	$V_{OUT} = 1V_{pp}$, 5MHz		61		dBc
e_n	Input Voltage Noise	> 1MHz		5		nV/ $\sqrt{\text{Hz}}$
i_n	Input Current Noise	> 1MHz, Inverting		20		pA/ $\sqrt{\text{Hz}}$
		> 1MHz, Non-Inverting		30		pA/ $\sqrt{\text{Hz}}$
X _{TALK}	Crosstalk	Channel-to-channel 5MHz		60		dB
DC Performance						
V _{IO}	Input Offset Voltage			0		mV
dV _{IO}	Average Drift			6		$\mu\text{V}/^\circ\text{C}$
I _{bn}	Input Bias Current - Non-Inverting			3		μA
dI _{bn}	Average Drift			40		nA/ $^\circ\text{C}$
I _{bi}	Input Bias Current - Inverting			6		μA
dI _{bi}	Average Drift			10		nA/ $^\circ\text{C}$
PSRR	Power Supply Rejection Ratio	DC		55		dB
A _{OL}	Open-Loop Transimpedance Gain	$V_{OUT} = V_S / 2$		TBD		k Ω
I _S	Supply Current	per channel		11		mA
Disable Characteristics - CLC3605 only						
T _{ON}	Turn On Time			55		ns
T _{OFF}	Turn Off Time			55		ns
OFF _{IOS}	Off Isolation	5MHz		TBD		dB
OFF _{COUT}	Off Output Capacitance			TBD		pF
OFF _{ROUT}	Off Output Resistance			TBD		k Ω
V _{OFF}	Power Down Input Voltage	DIS pin, disabled if pin is pulled above V _{OFF}	Disabled if DIS > 1.5V			V
V _{ON}	Enable Input Voltage	DIS pin, enabled if pin is grounded, left open or pulled below V _{ON}	Enabled if DIS < 0.5V			V
I _{SD}	Disable Supply Current	DIS pin is pulled to V _S		0.09		mA



Electrical Characteristics at +5V continued

$T_A = 25^\circ\text{C}$, $V_S = +5\text{V}$, $R_f = R_g = 330\Omega$, $R_L = 150\Omega$ to $V_S/2$, $G = 2$; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		150		$k\Omega$
		Inverting		70		Ω
C_{IN}	Input Capacitance			1.0		μF
CMIR	Common Mode Input Range			1.5 to 3.5		V
CMRR	Common Mode Rejection Ratio	DC		50		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		0.1		Ω
V_{OUT}	Output Voltage Swing	$R_L = 150\Omega$		1.5 to 3.5		V
I_{OUT}	Output Current			± 120		mA
I_{SC}	Short-Circuit Output Current	$V_{OUT} = V_S / 2$		± 130		mA

Notes:

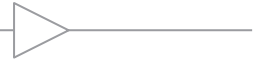
1. 100% tested at 25°C



Electrical Characteristics at $\pm 5V$

$T_A = 25^\circ C$, $V_S = \pm 5V$, $R_f = R_g = 330\Omega$, $R_L = 150\Omega$ to GND, $G = 2$; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	Unity Gain Bandwidth	$G = +1$, $V_{OUT} = 0.5V_{pp}$, $R_f = xxx\Omega$		TBD		MHz
BW _{SS}	-3dB Bandwidth	$G = +2$, $V_{OUT} = 0.5V_{pp}$		1400		MHz
BW _{LS}	Large Signal Bandwidth	$G = +2$, $V_{OUT} = 1V_{pp}$		650		MHz
BW _{0.1dBSS}	0.1dB Gain Flatness	$G = +2$, $V_{OUT} = 0.5V_{pp}$		120		MHz
BW _{0.1dBLS}	0.1dB Gain Flatness	$G = +2$, $V_{OUT} = 1V_{pp}$		TBD		MHz
Time Domain Response						
t_R , t_F	Rise and Fall Time	$V_{OUT} = 1V$ step; (10% to 90%)		1.5		ns
t_S	Settling Time to 0.1%	$V_{OUT} = 1V$ step		13		ns
OS	Overshoot	$V_{OUT} = 0.2V$ step		1		%
SR	Slew Rate	1V step		2500		V/ μ s
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	$V_{OUT} = 1V_{pp}$, 5MHz		-73		dBc
HD3	3rd Harmonic Distortion	$V_{OUT} = 1V_{pp}$, 5MHz		-73		dBc
THD	Total Harmonic Distortion	$V_{OUT} = 1V_{pp}$, 5MHz		69		dB
D _G	Differential Gain	NTSC (3.58MHz), DC-coupled, $R_L = 150\Omega$		0.02		%
D _P	Differential Phase	NTSC (3.58MHz), DC-coupled, $R_L = 150\Omega$		0.02		°
IP3	Third Order Intercept	$V_{OUT} = 0.5V_{pp}$, 10MHz		34		dBm
SFDR	Spurious Free Dynamic Range	$V_{OUT} = 1V_{pp}$, 5MHz		73		dBc
e_n	Input Voltage Noise	> 1MHz		5		nV/ \sqrt{Hz}
i_n	Input Current Noise	> 1MHz, Inverting		20		pA/ \sqrt{Hz}
		> 1MHz, Non-Inverting		30		pA/ \sqrt{Hz}
X _{TALK}	Crosstalk	Channel-to-channel 5MHz		60		dB
DC Performance						
V _{IO}	Input Offset Voltage ⁽¹⁾		-10	0	10	mV
dV _{IO}	Average Drift			6		μ V/ $^\circ C$
I _{bn}	Input Bias Current - Non-Inverting ⁽¹⁾		-35	3	35	μ A
dI _{bn}	Average Drift			40		nA/ $^\circ C$
I _{bi}	Input Bias Current - Inverting ⁽¹⁾		-35	6	35	μ A
dI _{bi}	Average Drift			10		nA/ $^\circ C$
PSRR	Power Supply Rejection Ratio ⁽¹⁾	DC	40	55		dB
A _{OL}	Open-Loop Transimpedance Gain	$V_{OUT} = V_S / 2$		TBD		k Ω
I _S	Supply Current ⁽¹⁾	per channel		12	18	mA
Disable Characteristics - CLC3605 only						
T _{ON}	Turn On Time			55		ns
T _{OFF}	Turn Off Time			55		ns
OFF _{IOS}	Off Isolation	5MHz		TBD		dB
OFF _{COUT}	Off Output Capacitance			TBD		pF
OFF _{ROUT}	Off Output Resistance			TBD		k Ω
V _{OFF}	Power Down Input Voltage	DIS pin, disabled if pin is pulled above V _{OFF}	Disabled if DIS > 3V			V
V _{ON}	Enable Input Voltage	DIS pin, enabled if pin is grounded, left open or pulled below V _{ON}	Enabled if DIS < 1V			V
I _{SD}	Disable Supply Current ⁽¹⁾	DIS pin is pulled to V _S		0.1	0.3	mA



Electrical Characteristics at $\pm 5V$ continued

$T_A = 25^\circ C$, $V_S = \pm 5V$, $R_f = R_g = 330\Omega$, $R_L = 150\Omega$ to GND, $G = 2$; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		150		$k\Omega$
		Inverting		70		Ω
C_{IN}	Input Capacitance			1.0		pF
CMIR	Common Mode Input Range			± 4.0		V
CMRR	Common Mode Rejection Ratio ⁽¹⁾	DC	40	50		dB
Output Characteristics						
R_O	Output Resistance	Closed Loop, DC		0.1		Ω
V_{OUT}	Output Voltage Swing	$R_L = 150\Omega$ ⁽¹⁾		± 4.0		V
I_{OUT}	Output Current			± 120		mA
I_{SC}	Short-Circuit Output Current	$V_{OUT} = V_S / 2$		± 290		mA

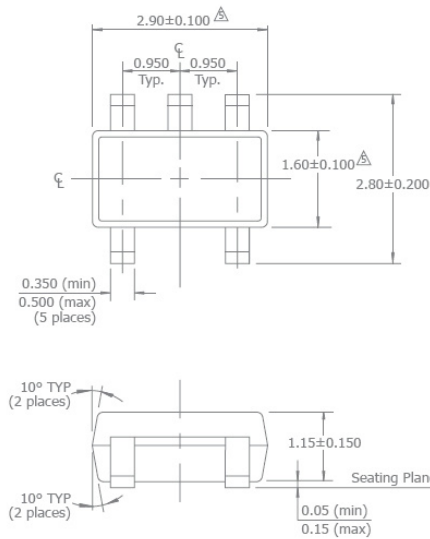
Notes:

1. 100% tested at $25^\circ C$



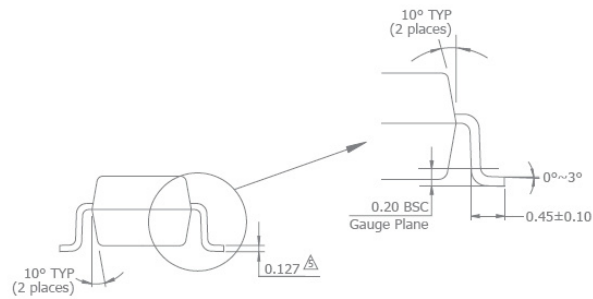
Mechanical Dimensions

SOT23-5 Package

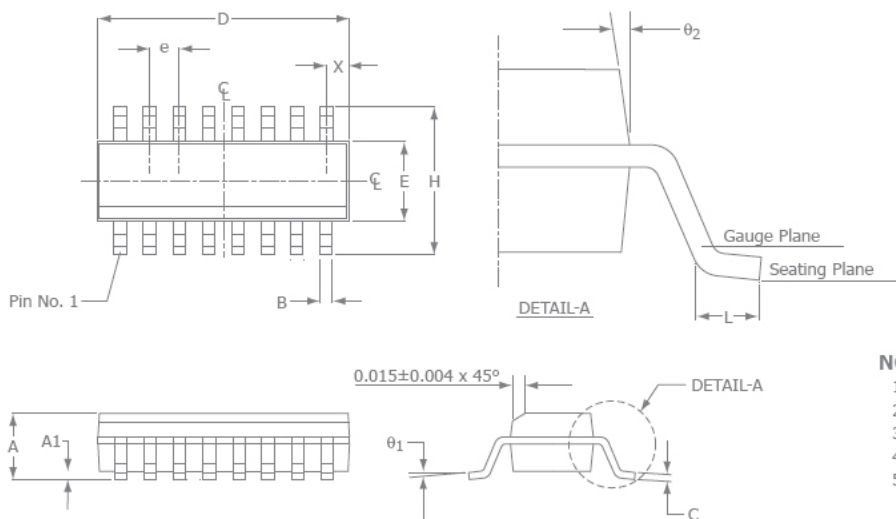


NOTES:

1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
 2. Package surface to be matte finish VDI 11~13.
 3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
 4. The footlength measuring is based on the gauge plane method.
- △ Dimension are exclusive of mold flash and gate burr.
 △ Dimension are exclusive of solder plating.



SOIC-16 Package



SOIC-16		
SYMBOL	MIN	MAX
A	0.054	0.068
A1	0.004	0.0098
B	0.014	0.019
D	0.386	0.393
E	0.150	0.157
H	0.229	0.244
e	0.050 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.020 Ref	
θ ₁	0°	8°
θ ₂	7° BSC	

NOTE:

1. All dimensions are in inches.
2. Lead coplanarity should be 0" to 0.004" max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.0075" from the lead tip.

For additional information regarding our products, please visit CADEKA at: cadeka.com

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