

AN-18

Competitor Replacement Guide for CDK8307



Introduction

The extreme low power of the CDK8307 is a large benefit to many ultrasound systems. The CDK8307 is pin compatible to several products on the market today. The CDK8307 can replace these devices in systems already in production, improving overall system power efficiency. This application note highlights any differences between CDK8307 and competition and lists the required modifications necessary to replace the competitive device with the CDK8307.

The following competitive products are reviewed:

- ADS5281 / ADS5282 - [Pages 1 thru 3](#)
- ADS5277 / ADS5287 - [Pages 4 thru 6](#)
- ADS5270 / ADS5271 / ADS5272 / ADS5273 - [Pages 7 thru 8](#)
- MAX1434 / MAX1436 / MAX1437 / MAX1438 / ADC12EU050 - [Pages 9 thru 10 \(additional information will be added later\)](#)
- AD9212 / AD9222 / AD9252 (An upcoming version of CDK8307 will be pin compatible, information will be added later)

ADS5281/ADS5282 vs. CDK8307C/CDK8307D

Comparison

Specification	CDK8307C	ADS5281	CDK8307D	ADS5282
#Channels /Resolution	Octal 12/14bit	Octal 12bit	Octal 12/14bit	Octal 12bit
Sampling Rate	50MSPS	50MSPS	65MSPS	65MSPS
SNR(dB) Typ Low Freq	72.2(8MHz)	70 (5MHz)	72.2(8MHz)	70 (5MHz)
SNR(dB) Minimum	71.1(8MHz)	68.3 (5MHz)	71.1(8MHz)	68.3 (5MHz)
SFDR(dB) Typ Low Freq	82(8MHz)	85 (5MHz)	82(8MHz)	85 (5MHz)
SFDR(dB) Minimum	75(8MHz)	74 (5MHz)	75(8MHz)	72 (5MHz)
Cross Talk (dB)	-95(9MHz)	-90	-95(9MHz)	-90
Active Power (mW)	321	530	382	616
Sleep Power (mW)	78	135	96	135
Pdwn Power (mW)	0.01	45	0.01	45
Startup from Sleep (us)	0.5	NA	0.5	NA
Startup from PDWN (us)	23	NA	23	NA
External Reference Decoupling	NONE	4cap 2 res	NONE	4cap 2 res
Output Type	LVDS	LVDS	LVDS	LVDS
Supply Voltage (V)	1.8 (1.7 to 3.6 for digital inputs)	3.3	1.8 (1.7 to 3.6 for digital inputs)	3.3

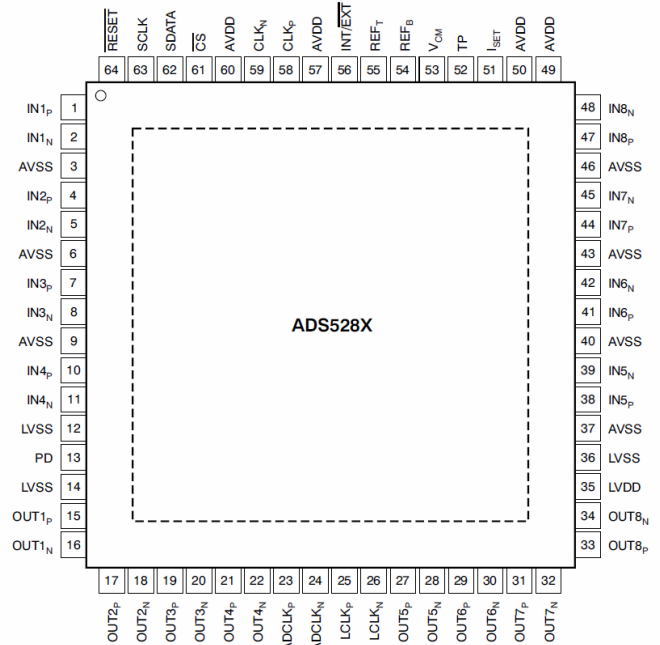
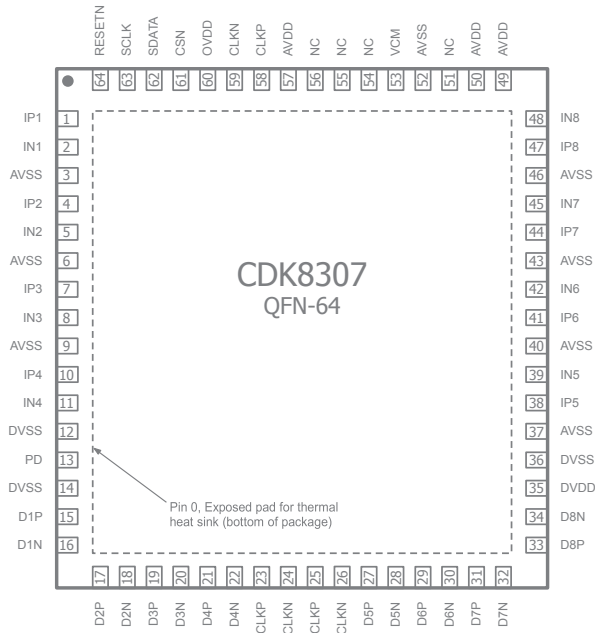
Ordering Information

CADEKA Part Number	Competitor Part Number	Package	Pin Compatible
CDK8307BITQ80	ADS5281IPFP	TQFP-80	Yes
CDK8307BILP64	ADS5281IRGC	QFN-64	Yes
CDK8307CILP64	ADS5282IRGC	QFN-64	Yes

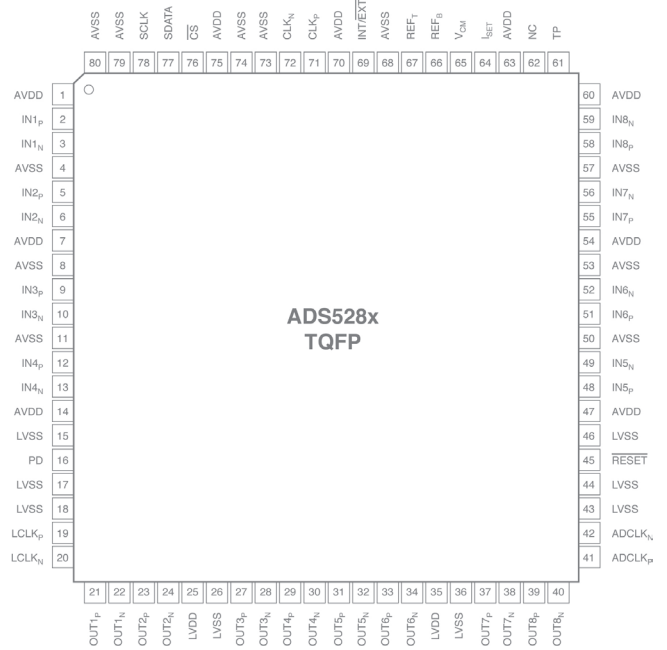
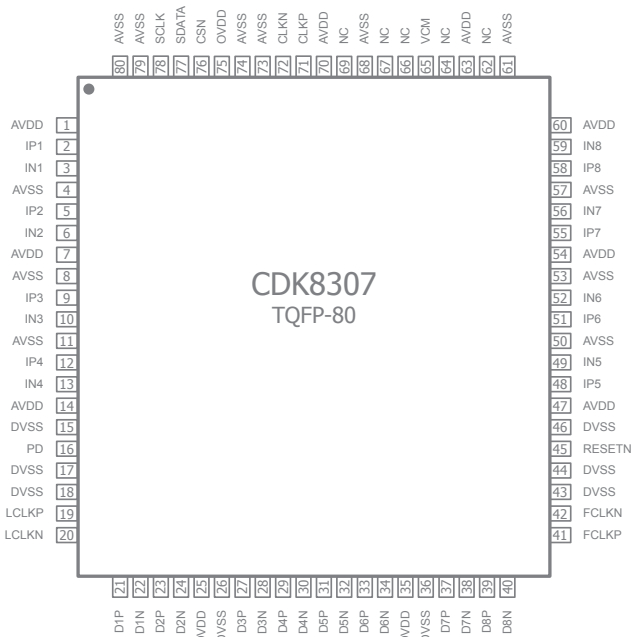


ADS5281/ADS5282 vs. CDK8307C/CDK8307D continued

QFN64 Pinout Diagram Comparison (Package Dimensions are Identical)



TQFP-80 Pinout Diagram Comparison (Package Dimensions are Identical)





ADS5281/ADS5282 vs. CDK8307C/CDK8307D continued

Major Differences

Specification	ADS518x	CDK8307x	CADEKA Benefit
Supply Voltage for analog supply	3.3V	1.7V to 2.0V	Lower Power
Supply Voltage for digital input drivers	3.3V	1.7V to 3.6V	
Supply Voltage for LVDS	1.8V	1.7V to 2.0V	Wider Tolerance
Input Common Mode Voltage	1.5V \pm 50mV	0.9V -100mV +200mV	
Common Mode Voltage Output (VCM)		AVDD/2 (typically 0.9V)	Fewer External Components Required
External Decoupling Capacitors on reference voltages	Required	Not Required (CDK8307 has internal references)	
Selection between single-ended (CMOS) and differential clock (LVDS, LVPECL, sine wave)	Requires a register setting	Does not require a register setting (For single-ended clock input, connect the negative clock input to GND)	Easier to Use
SPI Register Map	The main SPI register map is the same. However, some special functions are different.		More Options

Required Modifications for QFN Package

- Change AVDD supply voltage (pins 49 and 50) from 3.3V to 1.8V
- Adjust the digital supply, OVDD, (pin 60) from 1.7 to 3.6V. Ensure that this supply has the same voltage as the corresponding voltage level of a high CMOS input at pins 13, 61, 62, 63, and 64.
- Check that the input common mode voltage is correct. Most buffer amplifiers will do this automatically as the common mode output of CDK8307 has a different voltage compared to ADS528x. If the buffer amplifier does not support 0.9V common mode voltage, AC-coupling must be used. See the CDK8307 datasheet for details on AC-coupling.
- Double check that the used SPI register settings are relevant. In most cases the standard settings will work fine.

Required Modifications for TQFP Package

- Change AVDD supply voltage (pins 1, 7, 14, 47, 54, 60, 63, and 70) from 3.3V to 1.8V
- Adjust the digital supply, OVDD, (pin 75) from 1.7 to 3.6V. Ensure that this supply has the same voltage as the corresponding voltage level of a high CMOS input at pins 16, 45, 76, 77, and 78.
- Check that the input common mode voltage is correct. Most buffer amplifiers will do this automatically as the common mode output of CDK8307 has a different voltage compared to ADS528x. If the buffer amplifier does not support 0.9V common mode voltage, AC-coupling must be used. See the CDK8307 datasheet for details on AC-coupling.
- Double check that the used SPI register settings are relevant. In most cases the standard settings will work fine.



ADS5287/ADS5277 vs. CDK8307D

Comparison

The ADS5287 and ADS5277 are a 10-bit versions of ADS528x. Even at 10-bit resolution, these parts consume significantly more power than the CDK8307D. The lowest number of output bits that can be set up with the LVDS interface of the CDK8307 is 12. However, it is possible to use only the 10 most significant bits from the CDK8307. This can easily be done in the FPGA LVDS input circuitry.

Specification	CDK8307D	ADS5287	ADS5277
#Channels /Resolution	Octal 12/14bit	Octal 10bit	Octal 10bit
Sampling rate	65MSPS	65MSPS	65MSPS
SNR(dB) Typ Low Freq	72.2(8MHz)	61.7 (5MHz)	61.7 (5MHz)
SNR(dB) Minimum	71.1(8MHz)	60.5 (5MHz)	60.5 (5MHz)
SFDR(dB) Typ Low Freq	82(8MHz)	85 (5MHz)	85 (5MHz)
SFDR(dB) Minimum	75(8MHz)	72 (5MHz)	75 (5MHz)
Cross Talk (dB)	-95(9MHz)	-90	-89
Active Power (mW)	382	615	845
Sleep Power (mW)	96	135	92
Pdwn Power (mW)	0.01	45	NA
Startup from Sleep (us)	0.5	NA	NA
Startup from PDWN (us)	23	NA	NA
External Reference Decoupling	NONE	4cap 2 res	4cap 2 res
Output type	LVDS	LVDS	LVDS
Supply voltage (V)	1.8 (1.7 to 3.6 for digital inputs)	3.3	3.3

Ordering Information

CADEKA Part Number	Competitor Part Number	Package	Pin Compatible
CDK8307DILP64	ADS5287IRGC	QFN-64	Yes
CDK8307DITQ80	ADS5277IPFP	TQFP-80	Yes

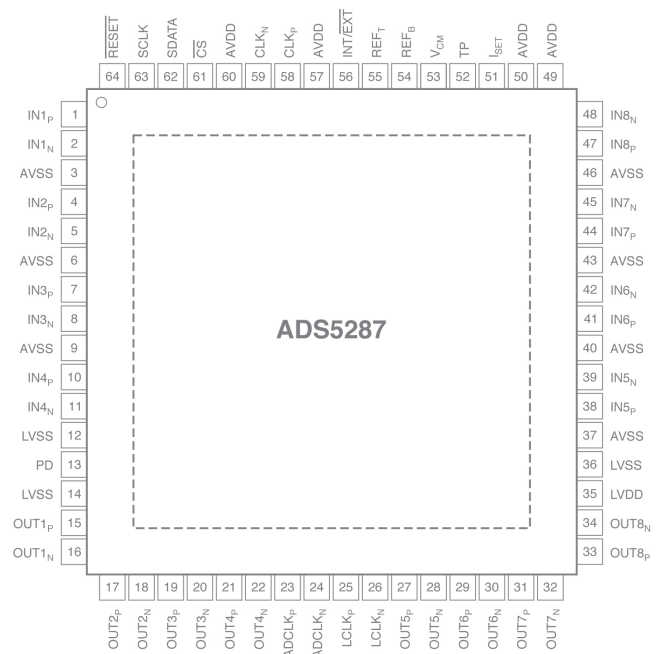
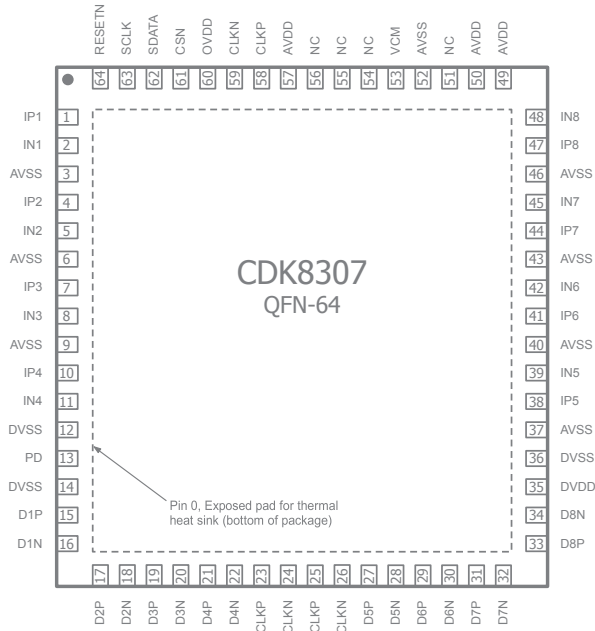
Major Differences

Specification	ADS5277 / ADS5287	CDK8307x	CADEKA Benefit
Supply Voltage for analog supply	3.3V	1.7V to 2.0V	Lower Power
Supply Voltage for digital input drivers	3.3V	1.7V to 3.6V	
Supply Voltage for LVDS	1.8V	1.7V to 2.0V	Wider Tolerance
Input Common Mode Voltage	1.5V ±50mV	0.9V -100mV +200mV	
Common Mode Voltage Output (VCM)		AVDD/2 (typically 0.9V)	Fewer External Components Required
External Decoupling Capacitors on reference voltages	Required	Not Required (CDK8307 has internal references)	
Selection between single-ended (CMOS) and differential clock (LVDS, LVPECL, sine wave)	Requires a register setting	Does not require a register setting (For single-ended clock input, connect the negative clock input to GND)	Easier to Use
SPI Register Map	The main SPI register map is the same. However, some special functions are different.		More Options

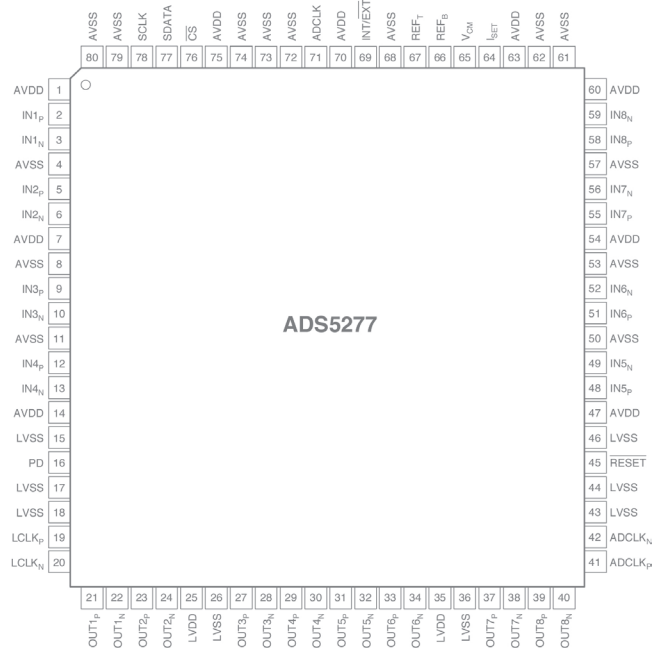
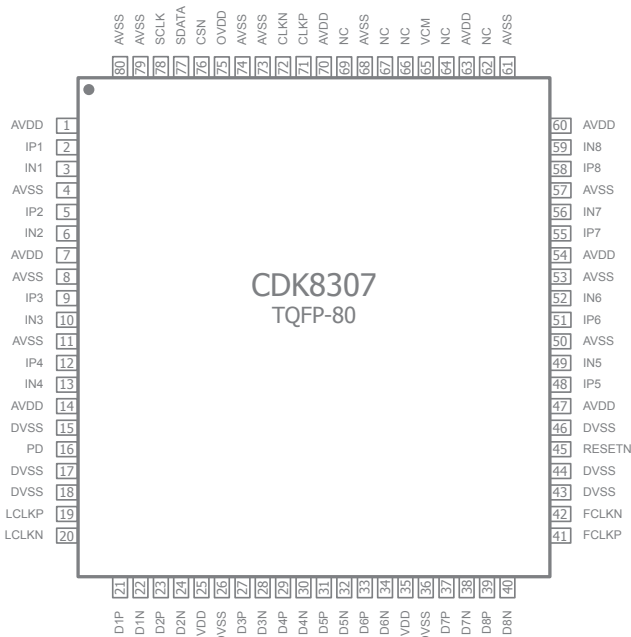


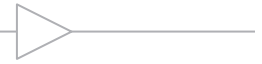
ADS5287/ADS5277 vs. CDK8307D continued

QFN64 Pinout Diagram Comparison (Package Dimensions are Identical)



TQFP-80 Pinout Diagram Comparison (Package Dimensions are Identical)





ADS5287/ADS5277 vs. CDK8307D continued

Required Modifications

- Change FPGA LVDS circuitry to receive 12 bits and use only the 10 most significant bits in further processing
- Change AVDD supply voltage (pins 49 and 50) from 3.3V to 1.8V
- Adjust the digital supply, OVDD, (pin 60) from 1.7 to 3.6V. Ensure that this supply has the same voltage as the corresponding voltage level of a high CMOS input at pins 13, 61, 62, 63, and 64.
- Check that the input common mode voltage is correct. Most buffer amplifiers will do this automatically as the common mode output of CDK8307 has a different voltage compared to ADS528x. If the buffer amplifier does not support 0.9V common mode voltage, AC-coupling must be used. See the CDK8307 datasheet for details on AC-coupling.
- Double check that the used SPI register settings are relevant. In most cases the standard settings will work fine.

Required Modifications for TQFP Package

- Change FPGA LVDS circuitry to receive 12 bits and use only the 10 most significant bits in further processing
- Change AVDD supply voltage (pins 1, 7, 14, 47, 54, 60, 63, and 70) from 3.3V to 1.8V
- Adjust the digital supply, OVDD, (pin 75) from 1.7 to 3.6V. Ensure that this supply has the same voltage as the corresponding voltage level of a high CMOS input at pins 16, 45, 76, 77, and 78.
- Check that the input common mode voltage is correct. Most buffer amplifiers will do this automatically as the common mode output of CDK8307 has a different voltage compared to ADS528x. If the buffer amplifier does not support 0.9V common mode voltage, AC-coupling must be used. See the CDK8307 datasheet for details on AC-coupling.
- Double check that the used SPI register settings are relevant. In most cases the standard settings will work fine.



ADS5270/71/72/73 vs. CDK8307A/B/C/D/E

Comparison

Specification	CDK8307A	CDK8307B	ADS5270	CDK8307C	ADS5271
#Channels /Resolution	Octal 12/14bit	Octal 12/14bit	Octal 12bit	Octal 12/14bit	Octal 12bit
Sampling rate	20MSPS	40MSPS	40MSPS	50MSPS	50MSPS
SNR(dB) Typ Low Freq	72.2(8MHz)	72.2(8MHz)	70.5 (5MHz)	72.2(8MHz)	70.5 (5MHz)
SNR(dB) Minimum	71.4(8MHz)	71.4(8MHz)	68 (5MHz)	71.1(8MHz)	69.5 (5MHz)
SFDR(dB) Typ Low Freq	82(8MHz)	82(8MHz)	87 (5MHz)	82(8MHz)	87 (5MHz)
SFDR(dB) Minimum	75(8MHz)	75(8MHz)	78 (5MHz)	75(8MHz)	78 (5MHz)
Cross Talk (dB)	-95(9MHz)	-95(9MHz)	-90	-95(9MHz)	-90
Active Power (mW)	175	272	888	321	927
Sleep Power (mW)	43	67	90	78	92
Pdwn Power (mW)	0.01	0.01	NA	0.01	NA
Startup from Sleep (us)	0.5	0.5	NA	0.5	NA
Startup from PDWN (us)	23	23	NA	23	NA
External Reference Decoupling	NONE	NONE	4cap 2 res	NONE	4cap 2 res
Output type	LVDS	LVDS	LVDS	LVDS	LVDS
Supply voltage (V)	1.8 (1.7 to 3.6 for digital inputs)	1.8 (1.7 to 3.6 for digital inputs)	3.3	1.8 (1.7 to 3.6 for digital inputs)	3.3

Comparison continued

Specification	CDK8307D	ADS5272	CDK8307E	ADS5273
#Channels /Resolution	Octal 12/14bit	Octal 12bit	Octal 12bit	Octal 12bit
Sampling rate	65MSPS	65MSPS	80MSPS	70MSPS
SNR(dB) Typ Low Freq	72.2(8MHz)	71.1 (5MHz)	70.3(8MHz)	71.1 (5MHz)
SNR(dB) Minimum	71.1(8MHz)	69 (5MHz)	69.2(8MHz)	69 (5MHz)
SFDR(dB) Typ Low Freq	82(8MHz)	89 (5MHz)	77(8MHz)	90 (5MHz)
SFDR(dB) Minimum	75(8MHz)	77 (5MHz)	74(8MHz)	76 (5MHz)
Cross Talk (dB)	-95(9MHz)	-89	-95(9MHz)	-89
Active Power (mW)	382	983	445	1003
Sleep Power (mW)	96	94	105	95
Pdwn Power (mW)	0.01	NA	0.05	NA
Startup from Sleep (us)	0.5	NA	0.25	NA
Startup from PDWN (us)	23	NA	12	NA
External Reference Decoupling	NONE	4cap 2 res	NONE	4cap 2 res
Output type	LVDS	LVDS	LVDS	LVDS
Supply voltage (V)	1.8 (1.7 to 3.6 for digital inputs)	3.3	1.8 (1.7 to 3.6 for digital inputs)	3.3

Ordering Information

CADEKA Part Number	Competitor Part Number	Package	Pin Compatible
CDK8307BITQ80	ADS5270IPFP	TQFP-80	Yes
CDK8307CITQ80	ADS5271IPFP	TQFP-80	Yes
CDK8307DITQ80	ADS5272IPFP	TQFP-80	Yes
CDK8307EITQ80	ADS5273IPFP	TQFP-80	Yes



MAX1436 vs. CDK8307B

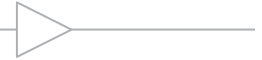
Comparison

Specification	CDK8307B	MAX1436	MAX1436B
#Channels /Resolution	Octal 12/14bit	Octal 12bit	Octal 12bit
Sampling rate	40MSPS	40MSPS	40MSPS
SNR(dB) Typ Low Freq	72.2(8MHz)	69.9 (5.3MHz)	69.9 (5.3MHz)
SNR(dB) Minimum	71.4(8MHz)	66.5 (19MHz)	66.5 (19MHz)
SFDR(dB) Typ Low Freq	82(8MHz)	96 (5.3MHz)	96 (5.3MHz)
SFDR(dB) Minimum	75(8MHz)	79 (19MHz)	79 (19MHz)
Cross Talk (dB)	-95(9MHz)	-85	-85
Active Power (mW)	272	743	743
Sleep Power (mW)	67	NA	60
Pdwn Power (mW)	0.01	3.5	NA
Startup from Sleep (us)	0.5	NA	200
Startup from PDWN (us)	23	100000	NA
External Reference Decoupling	NONE	1cap 2 res	1cap 2 res
Output type	LVDS	LVDS	LVDS
Supply voltage (V)	1.8 (1.7 to 3.6 for digital inputs)	1.8	1.8

MAX1434 / MAX1437B / ADC12EU050 vs. CDK8307C

Comparison

Specification	CDK8307C	MAX1437B	MAX1434	ADC12EU050
#Channels /Resolution	Octal 12/14bit	Octal 12bit	Octal 10bit	Octal 12bit CT-DS
Sampling rate	50MSPS	50MSPS	50MSPS	50MSPS
SNR(dB) Typ Low Freq	72.2(8MHz)	70.2 (5.3MHz)	61.1 (5.3MHz)	69.3 (4.4MHz)
SNR(dB) Minimum	71.1(8MHz)	67 (19MHz)	60 (19MHz)	62.1 (4.4MHz SINAD)
SFDR(dB) Typ Low Freq	82(8MHz)	98 (5.3MHz)	84 (5.3MHz)	77 (4.4MHz)
SFDR(dB) Minimum	75(8MHz)	79 (19MHz)	77 (19MHz)	66 (4.4MHz)
Cross Talk (dB)	-95(9MHz)	-75	-94	??
Active Power (mW)	321	759	767	385
Sleep Power (mW)	78	60	NA	40
Pdwn Power (mW)	0.01	NA	3.5	5
Startup from Sleep (us)	0.5	200	NA	12
Startup from PDWN (us)	23	NA	100000	18000
External Reference Decoupling	NONE	1cap 2 res	1cap 2 res	2cap 1res
Output type	LVDS	LVDS	LVDS	LVDS
Supply voltage (V)	1.8 (1.7 to 3.6 for digital inputs)	1.8	1.8	1.8



MAX1438 vs. CDK8307D

Comparison

Specification	CDK8307D	MAX1438
#Channels /Resolution	Octal 12/14bit	Octal 12bit
Sampling rate	65MSPS	65MSPS
SNR(dB) Typ Low Freq	72.2(8MHz)	69.9 (5.3MHz)
SNR(dB) Minimum	71.1(8MHz)	66.5 (19MHz)
SFDR(dB) Typ Low Freq	82(8MHz)	95 (5.3MHz)
SFDR(dB) Minimum	75(8MHz)	79 (19MHz)
Cross Talk (dB)	-95(9MHz)	-85
Active Power (mW)	382	913
Sleep Power (mW)	96	NA
Pdwn Power (mW)	0.01	3.5
Startup from Sleep (us)	0.5	NA
Startup from PDWN (us)	23	100000
External Reference Decoupling	NONE	1cap 2 res
Output type	LVDS	LVDS
Supply voltage (V)	1.8 (1.7 to 3.6 for digital inputs)	1.8

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