CADEKA
Amplify the Human Experience

# AN-15

## CEB3404 Evaluation Board for CDK3404
## 8-bit, 180 MSPS, Triple Video DAC



### FEATURES

- Up to 180 MWPS Conversion Rate
- Reference Voltage Circuit
- Standard Video BNC Connectors for DAC Outputs
- Data and Clock Buffers
- Clock and Data Monitor Test Points
- Clock, Sync and Blank Inputs Selectable for 0 or 180 Degree Phase
- Option to add CLC3800/CLC3801 Triple Video Filter

### APPLICATIONS

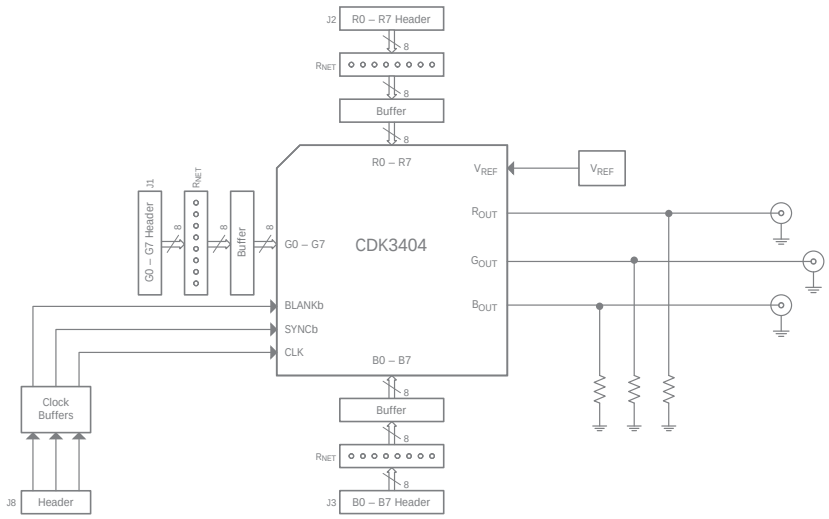
- Evaluation of the CDK3404 Video DAC
- RGB Video Generator
- Standard Definition Video Filter Option
- Guide to PCB Layout
- Guide to Design with the CDK3404
- Guide to Design with the CLC3800/CLC3801

## General Description

The CEB3404 evaluation board is intended as a tool for device evaluation and characterization and to demonstrate the performance of the CDK3404 (8-bit, 180 MWPS Triple Video DAC). The CEB3404 will accept up to 8-bit binary input words into each of the three DAC inputs. These data signals are buffered by a 10-bit buffer. (Note: The lower two bits should be tied to ground with jumpers at each of the three header inputs.) A single input clock and two control signals (SYNCb and BLANKb) are also buffered using dual input XOR gates. This allows for easy phase inversion of these signals if timing control is required. The digital input data for all three DACs is latched into the CDK3404 on the rising edge of the clock input signal. The output current is determined by an external resistor which sets a reference current based upon the device reference voltage $V_{REF}$. $V_{REF}$ is generated internal to the CDK3404, or optionally can be generated externally and applied to the $V_{REF}$ input. Output current is converted to an output voltage with a ground referenced 75Ω external resistor. Output levels can be overridden by the two control signals (SYNCb and BLANKb) to insert the required video synchronization signals.

This application note is a supplement to the CDK3404 datasheet and is intended to provide more applications detail with respect to: power supplies and grounding, logic interface circuits, external voltage reference circuits and specific layout issues.

## Block Diagram



## Power Supplies and Grounding

The CEB3404 requires two separate +3.3V power supplies. One for the digital circuitry which includes the input and clock buffers, and one for the analog circuitry which includes the CDK3404, external reference circuit and the optional CLC3800 video filter option. The CLC3800 option can be powered from either the board analog supply, or if desired from an additional separate power terminal. Adequate decoupling of both supplies is incorporated into the design. However, use of low-noise (non-switching) regulated supplies with low source impedance is recommended.

The power return and grounding connections are accomplished with a split ground plane, one for the digital return and one for the analog return. The two ground planes are coupled together through an inductive ferrite bead (L1) near the DAC. The purpose of this connection is to keep the high-speed digital switching signal noise from entering the low-noise analog section.

## Reference Circuits

The CDK3404 provides an on-board voltage reference of 1.25V, and can be accessed at the test point labeled REF_TP. The internal reference requires an external 0.1uF compensation capacitor, which is installed between the COMP (pin34) and the positive analog supply.

For higher accuracy, the CEB304 also contains an external reference voltage source that can be accessed through jumper J7. If connected, the external reference will override and take precedence over the internal reference of the CDK3404 and appear at REF_TP. The required 0.1uF VREF decoupling capacitor is present for both configurations.

The CEB3404 reference consists of an integrated two-terminal band-gap reference diode, LT1004. The typical output at 100uA bias is 1.235V ± 4mV. The reference diode is biased to the analog supply with a 3.3KΩ resistor, setting a bias current of 1.136mA.

Reference currents for the DAC are derived from $V_{REF}$ through a current setting resistor, R41 attached between $R_{REF}$ (P36) and analog ground. The full-scale output current of each DAC is a multiple of this value, so a low tolerance, ceramic thin-film resistor is used. The nominal value for $R_{REF}$ can be derived from:

$R_{REF} = 5.31 (V_{REF}/I_{FS})$

where $I_{FS}$ is the desired full-scale output current.

$I_{FS}$ is determined by the required full-scale output voltage divided by the DAC resistive load:

$I_{FS} = V_{FS} / R_{LOAD}$

Figure 1 below shows a single DAC driving a typical 75Ω video load over a 75Ω transmission line. To reduce transmission reflections, an additional back-matching 75Ω resistor is used. This appears in parallel with the video load for an effective load resistance of 37.5Ω.

So, from above, with a standard full-scale video level (WHITE) of 700mV, sets $I_{FS}$ = 700mV/37.5Ω = 18.67mA.

And so $R_{REF}$ = 5.31 (1.235V/18.67mA) = 355.6Ω. To ensure adequate output levels, this is rounded down to the next standard resistor size of 348Ω.

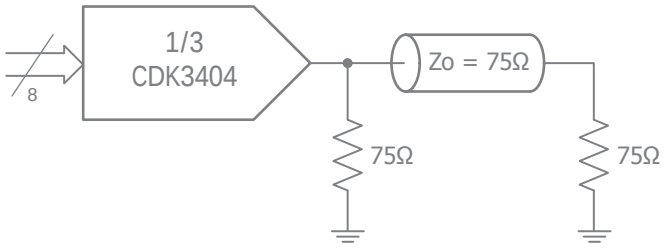



Figure 1. Typical DAC Connection

## Video Data and Timing Circuits

Digital RGB data is brought on-board through three separate 20-Pin headers (J1-J3). Each of the 10 input bits for each convertor has an associated ground return pin. As the CDK3404 is an 8-bit device, the lower two bits for each DAC are tied to ground potential with a jumper at the header input. The data passes through 10-bit TTL buffers before being presented to the CDK3404. Pull-up resistors are present on all inputs to ensure fixed levels if the inputs are left floating.

The CEB3404 evaluation board accepts three separate timing clocks, CLOCK, BLANKb and SYNCb. Please refer to the datasheet for a more detailed description of their functions. The timing inputs are all located on the J8 header connector. Ground return connections for all three clocks are available on J19.

The clocks are all buffered using a 74F86 Exclusive-OR gate. This not only helps to match the delay of the data input buffers, but also allows for a 180° phase inversion. This may be useful when interfacing to additional clocked systems, such as an upstream digital video processor.

All three DAC's capture and convert their respective input data with the same clock. Data is latched into the CDK3404 on the rising edge of its clock input. Analog outputs follow after a delay, $t_D$ from rising edge. For the CEB3404 evaluation board, the system clock is input on the J8 header.

Refer to the datasheet for specific timing information such as data set-up and hold times and minimum clock pulse widths.

It is important that negative transients are not introduced onto the data or clock inputs. To alleviate this, 22Ω resistors are placed in series with all inputs to reduce the current injection from high slew rate edges.

## Analog Outputs

The three RGB outputs are comprised of variable, ground-referenced current sources. To create an output voltage, these currents drive a resistor tied between the output and analog ground. As mentioned in the REFERENCE CIRCUITS section above, this voltage is dependent upon three factors: Effective output load resistance, Absolute value of the reference voltage ($V_{REF}$) and the value of the $R_{SET}$ resistor. Although designed for standard video levels of 700mV with additional 300mV headroom for sync signals, the outputs can range anywhere within the allowable compliance range. Typical output load is expected to be 37.5Ω. If lower values are used, please ensure that the maximum current output ratings are not exceeded.

The CEB3404 is configured with a fixed, low tolerance 75Ω load resistor on each output. It is expected that the user will attach the outputs to an external standard 75Ω video load via the output BNC connectors. Failure to properly terminate the outputs will result in twice the expected output voltage swing.

## CLC3800/CLC3801 Option – Triple Standard Definition Video Reconstruction Filter

If desired, the CEB3404 can be configured with a CLC3800 or CLC3801 video reconstruction filter. With this option, the CLC3800/01 and associated decoupling capacitors are added to the bottom side of the board. Removal of jumpers J26, J27 and J28 are required to isolate the outputs of the CDK3404 from the outputs of the CLC3800. In this configuration, the outputs of the CDK3404 are available at the R, G and B test points and the outputs of CLC3800/01 are routed to the output BNC connectors.

**NOTE:** If using this option, ensure that the jumpers remain disconnected to ensure isolation of the DAC and FILTER outputs.

The CLC3800 provides 6dB of gain as well as a 4th order 8MHz Butterworth low-pass filter. A 75Ω series back-matching resistor is included for driving a standard doubly-terminated load. As with the CDK3404, an external 75Ω video load is expected to provide proper video levels. Outputs can be either DC or AC coupled.

The CLC3801 is configured is the same fashion except it provides +9dB of gain.

Power connection for the CLC3800/3801 can be tied to the same analog supply used by the CDK3404 through jumper J30. In addition, as the CLC3800/3801 can operate down to a 3V supply, a separate power connection is available to help demonstrate the low power operation of the CLC3800/3801.

## PCB Layout

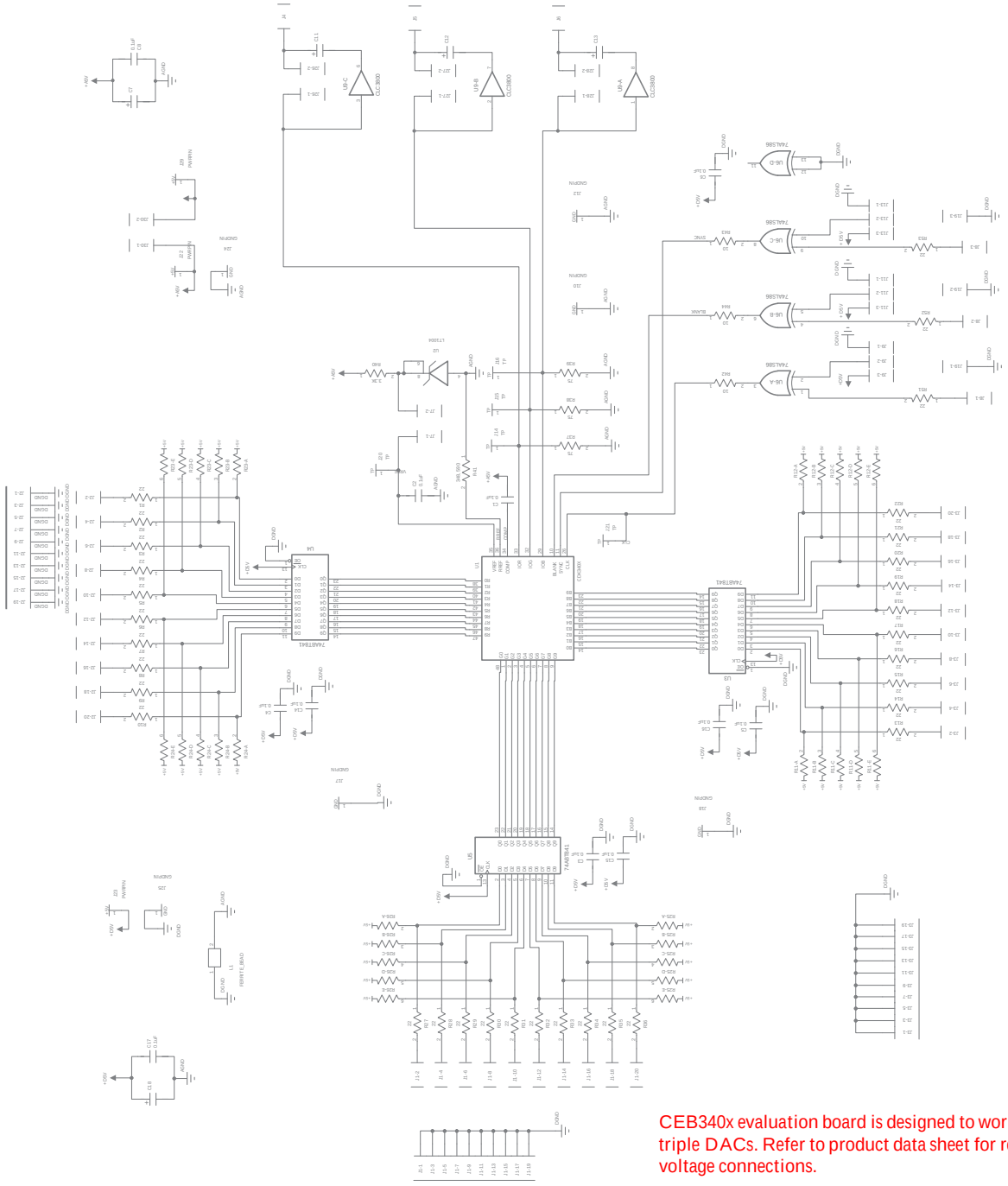
Careful consideration of the layout of this evaluation board was performed by CADEKA to ensure maximum performance for the part and to aid users in developing similar designs and layout aspects. Some highlights of the CEB3404 layout are as follows.

- The ground plane is split into analog and digital planes. They are tied together at only one point through a ferrite bead (L1). This connection reduces the amount of digital switching noise being induced into the analog output.
- Separate supplies are used for digital and analog circuitry. All buffers and clock circuits run from the digital supply. The CDK3404 and the reference source are powered from the analog supply.

  If a single supply is desired, an additional ferrite bead should be used to help isolate digital switching noise from entering the analog rail used for the CDK3404. In this configuration, separate supply decoupling capacitors should be used on each rail and terminated to their respective ground plane.

- This evaluation board contains both energy storage and high frequency bypass power supply decoupling capacitors.
- Controlled impedance signal traced and associated termination of signals should be considered when operating this device at maximum conversion rates. This is necessary to minimize energy reflections from contaminating signals, especially at high slew and repetition rates. Sockets for SIP resistor or RC networks have been provided. A series termination resistor has been provided for each clock signal.
- Undershoot transients are kept within limits for this evaluation board by using buffers in front of and in close proximity to the CDK3404.





CEB340x evaluation board is designed to work with several CADEKA triple DACs. Refer to product data sheet for recommended supply voltage connections.

CDK3404 does not use 5V supply, refer to CDK3404 data sheet.

Figure 2. CEB3404 Schematic Diagram

Table I – CEB340x Evaluation Board for CDK3404 - Bill of Materials

| # | Reference | Manufacturer Part Number | Description | Qty | Suggested Manufacturer |
|---|---|---|---|---|---|
| 1 | U1 | CDK3404 | Triple DAC | 1 | CADEKA |
| 2 | U3,U4,U5 | SN74ABT841ADWR | 10B Transparent Latch | 3 | Texas Inst. |
| 3 | U2 | LT1004CDR-1-2 | 1.235V Voltage Reference | 1 | Texas Inst. |
| 4 | R11,R12,R23-R26 | 77061472P | Res Net 5Res 4.7kΩ 6-pin | 6 | CTS |
| 5 | U6 | SN74F86DR | IC Quad 2-In EX-OR Gate | 1 | Texas Inst. |
| 6 | L1 | EXC-ELSA35 | Bead Core Single 3.5x5mm Axial | 1 | Panasonic |
| 7 | J4,J5,J6 | 31-71047-1010 | Conn BNC PC Mt Rt/Ang 75Ω | 3 | Amphenol-RF |
| 8 | J1,J2,J3 | | 2x10 Header - Right Angle | 3 | |
| 9 | J8,J9,J11,J13,J19 | | 1x3 Header - Straight | 5 | |
| 10 | J7,J26,J27,J28 | | 1x2 Header - Straight | 4 | |
| 11 | R3-R10,R15-R22, R29-R36 | | 22Ω Resistor/5%/50V | 30 | |
| 12 | R37,R38,R39 | | 75Ω Resistor/1%/50V | 3 | |
| 13 | R41 | | 348Ω Resistor/1%/50V | 1 | |
| 14 | R40 | | 3.3kΩ Resistor/5%/50V | 1 | |
| 15 | C1-C6, C8, C14-C17 | ECJ-2YB1H104K | Cap 0.1µF 50V Ceramic x7r 0805 | 7 | Panasonic |
| 16 | C7, C18 | TAJB106K020R | Cap Tantalum 10µF 20V 10% Smd | 1 | AVX |
| 17 | J22,J23 | 5010 | Red Power Connection Pins | 2 | Keystone |
| 18 | J10,J12,J17,J18, J24,J25 | 5011 | Black Power Connection Pins | 6 | Keystone |
| 19 | J14,J15,J16,J20,J21 | 5002 | Test Points | 5 | Keystone |
| 20 | R42-44, R51-53 | | 0Ω Resistor/5%/50V | 6 | |
| * | C9 | | 0.1µF Capacitor NC | n/a | |
| * | C10 | | 6.8µF Capacitor NC | n/a | AVX |
| * | C11,C12,C13 | | 220µF Capacitor NC | n/a | AVX |
| * | U9 | CLC3800 | 3-Channel Video Filter NC | n/a | CADEKA |
| * | J30 | 5010 | Red Power Connection Pins NC | n/a | Keystone |

**NOTE:**

* These parts are for the CLC3800 video filter option. Not implemented unless special ordered.
** R1,R2,R13,R14,R27,R28 are not used.

## Evaluation Board Layout

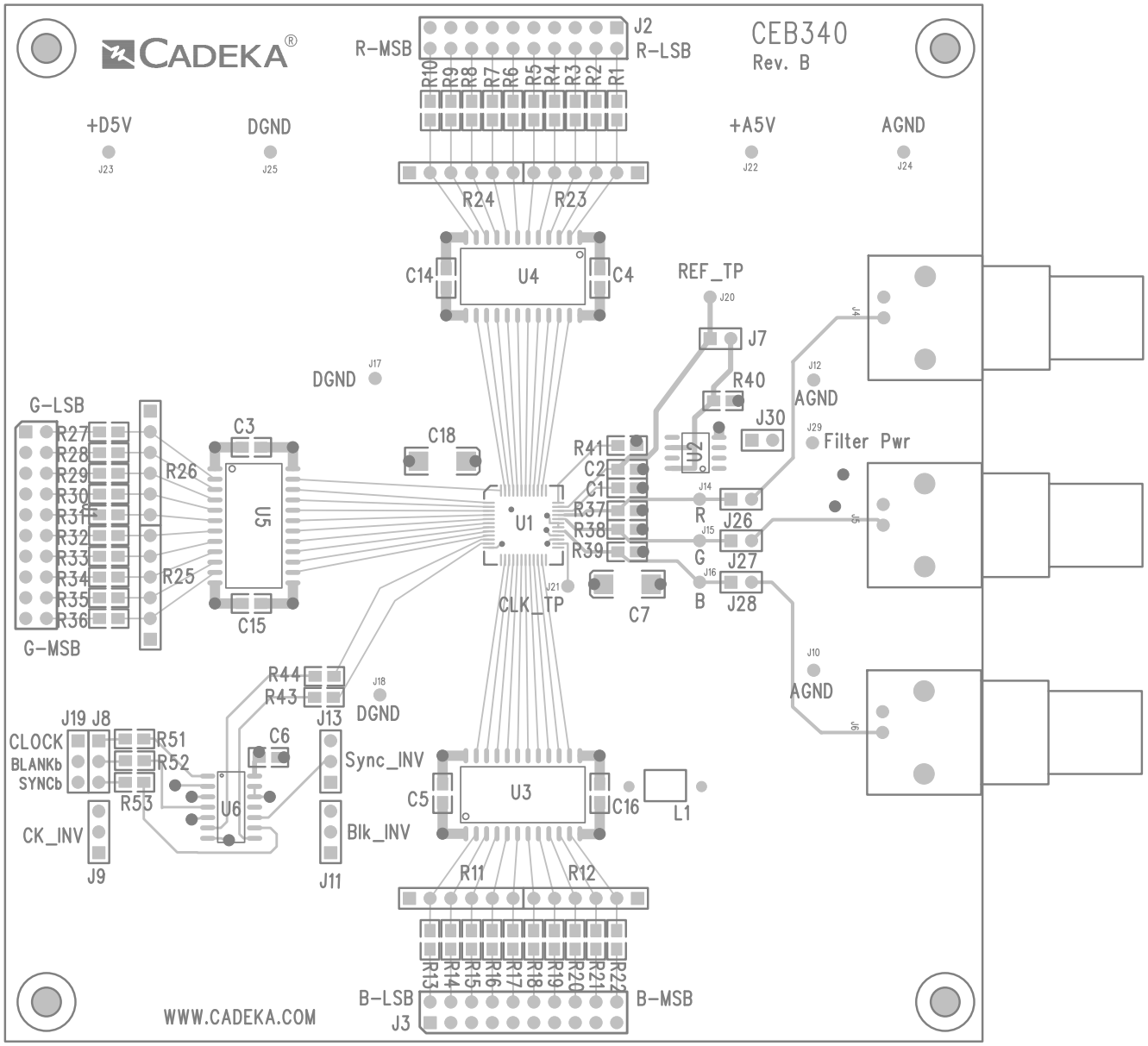



Figure 3. CEB3404 Top Side Board Layer

CEB340x evaluation board is designed to work with several CADEKA triple DACs. Refer to product data sheet for recommended supply voltage connections.

CDK3404 does not use 5V supply, refer to CDK3404 data sheet.

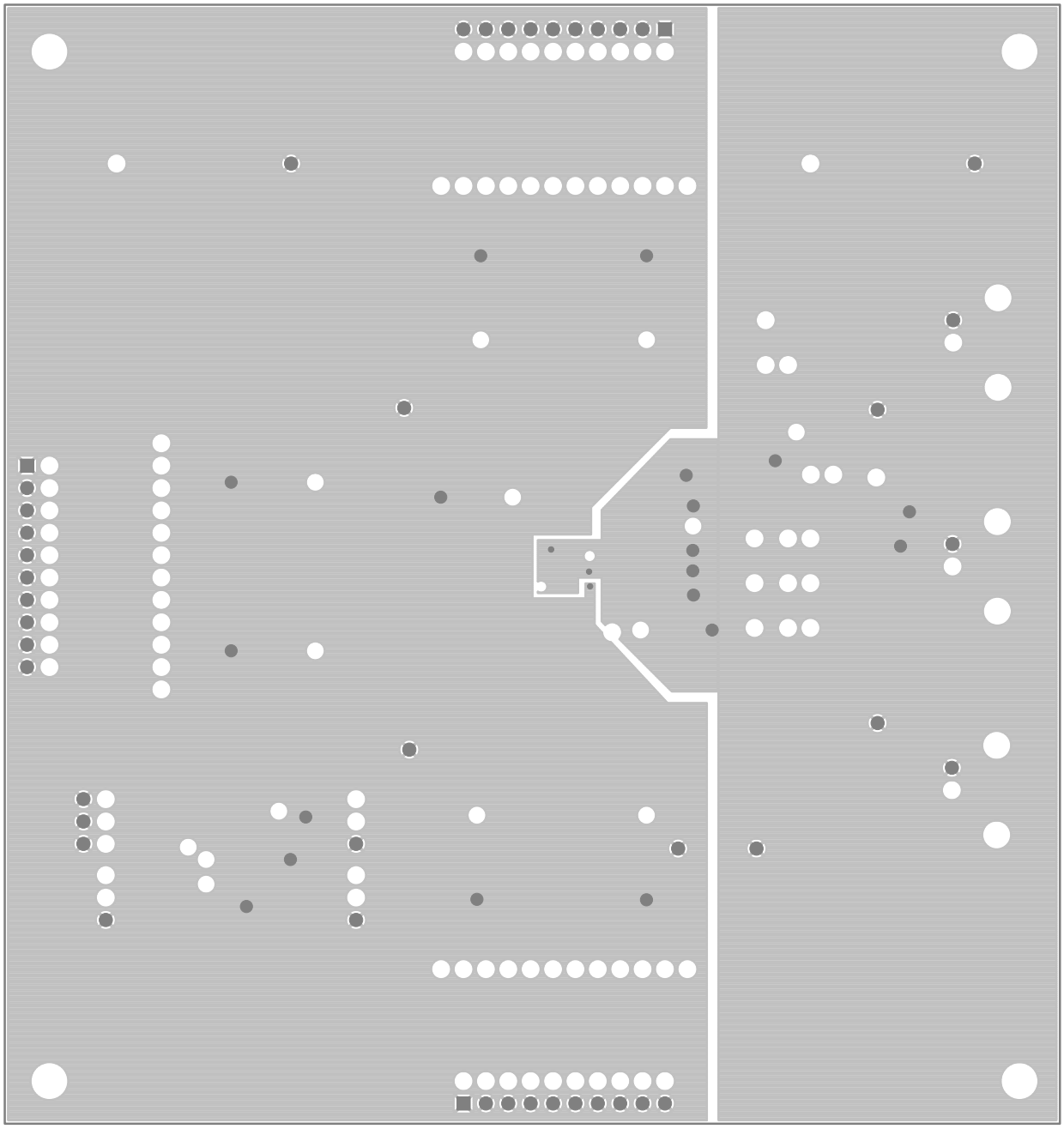


Figure 4. CEB3404 GND Side Board Layer

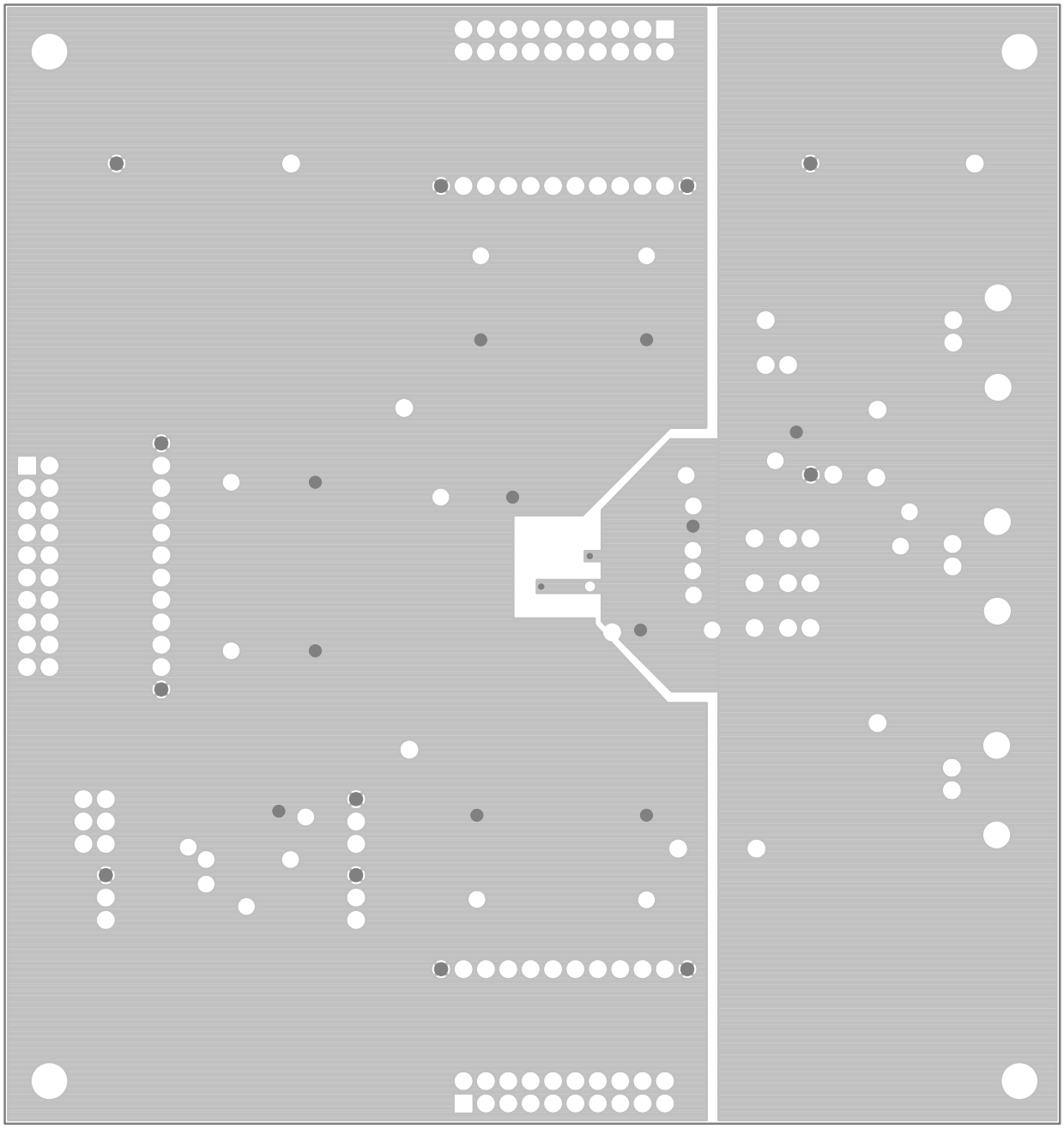


Figure 5. CEB3404 PWR Side Board Layer

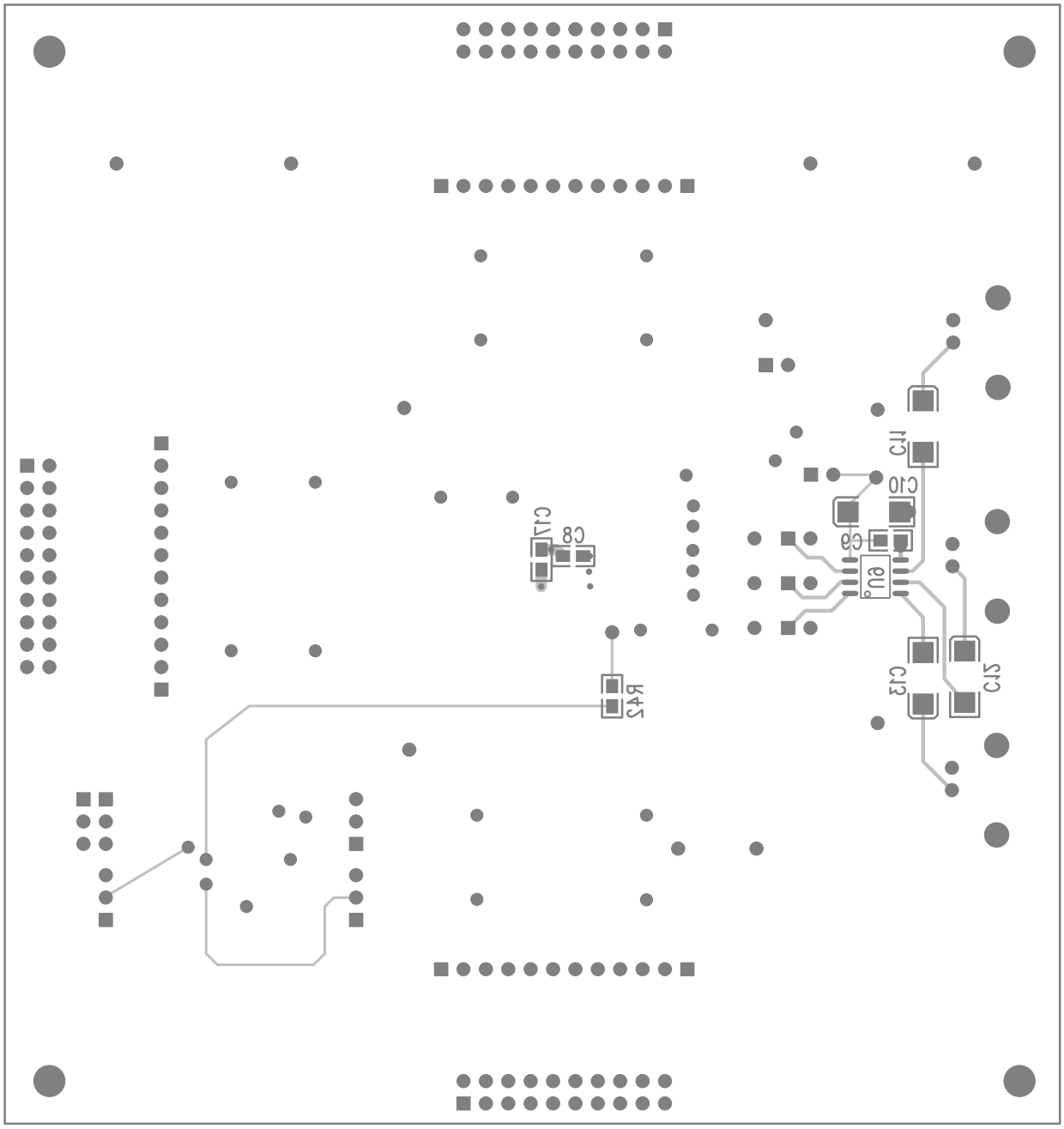



Figure 6. CEB3404 Bottom Side Layer